INTERNATIONAL RESEARCH JOURNAL OF MULTIDISCIPLINARY TECHNOVATION (IRJMT)

http://www.mapletreejournals.com/index.php/IRJMT
Received 21 May 2019 ISSN 2582-1040
Accepted 24 May 2019 2019; 1(3); 40-47
Published online 25 May 2019

DESIGN OF SOLAR PV BASED SHUNT ACTIVE FILTER FOR NONLINEASR LOAD

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DOI: https://doi.org/10.34256/irjmt1935

ABSTRACT

Elevation of power electronics technology, converter are the main causes for power quality issues, because of their high switching characteristics.so to reduce the harmonics injected by the nonlinear load, the filters are play a major role to improve a power quality improvement, particularly shunt active filter is more reliable for reduce a harmonic in power system network. This novel technique proposed for design a shunt active filter with solar photovoltaic array integrated into nonlinear load using a Point of Common Coupling (PCC) technique. Zero crossing detection technique are used to extract the magnitude of a fundamental active components of distorted load currents. The estimation of harmonic isolator and current compensation are controlled by Field Programmable Gate Array (FPGA) controller, different types of compensation techniques are used in this work Synchronous reference frame theory, instantaneous reactive power theory (PQ) and hysteresis current control technique. These techniques enable extraction of active power, regulates a load voltage and maintain a phasor sequence at PCC under the voltage sag and swell. Simulation is carried out by MATLAB/SIMULINK for different compensations techniques and Total Harmonics Distortion (THD) values are tabulated.

Keywords: Field Programmable Gate Array (FPGA), Photovoltaic (PV), Point of Common Coupling (PCC)

1. INTRODUCTION

In recent years, due to the modernizing and interfacing of renewable energy sources, the usage of power converters in the utility grid has been increased. These loads inject the harmonics into the power grid, since they reveal the nonlinear characteristics. The deviation in the power supplied to any electrical equipment from its steady, sinusoidal 50/60 Hz voltage or current may cause disturbance to the safe and reliable operation of the power system. This will also lead to malfunctioning of the equipment and even their failure. Particularly, harmonics cause more problems such as overheating, excessive neutral current in three phase four wire system, low power factor, and consumption of reactive power. Among the different nonlinear loads, the practice of using Switch Mode Power Supply (SMPS) is quite common in industrial as well as commercial applications, which involves the usage of various types of AC – DC converters and they are considered in this section to study the effect of nonlinearity.

2. MODELLING OF SHUNT ACTIVE POWER FILTER

The modern countries 50-60% of electric power flow is through the power electronic systems. Due to the advancement in power electronic technology, the percentage of usage of power electronic devices is growing in nature. The nonlinear characteristics of the power electronic devices affect the quality of the power by introducing harmonics in the system. The harmonics have subsequent effects on the grid parameters as well as equipment connected to the grid.

2.1. Working principle of SAPF

SAPF is connected in parallel to the grid at PCC, in order to inject the compensating current with the same magnitude of the load current and opposite phase into the system. Irrespective of the load type, this principle can be applied to achieve the harmonics free source current (Singh et al. 1999). In addition to this it compensates the reactive power requirement of the load, voltage harmonics and balancing the system (El-Habrouk et al. 2000). The block diagram of SAPF is shown in the Figure 2.1.

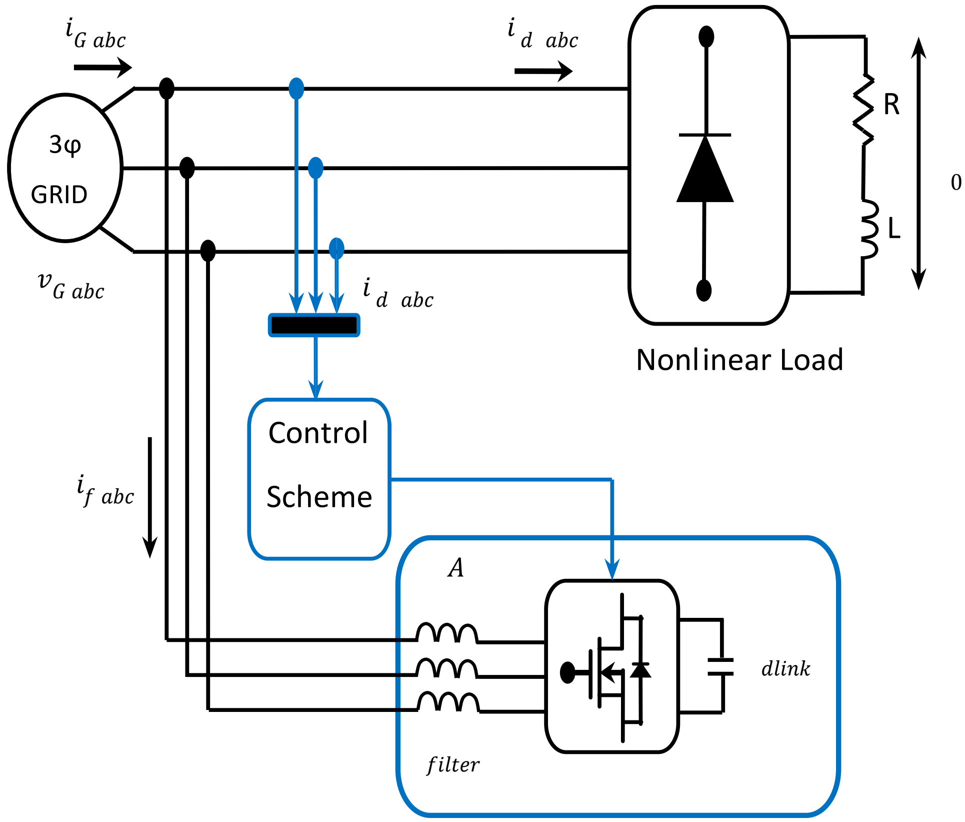

Fig 2.1 Block diagram of SAPF

2.2. Modelling of SAPF

SAPF is implemented by using the standard three phase VSI along with the output filter inductor. Figure 2.2. represents the circuit topology of VSI based three phase SAPF connected to the three phase balanced grid. Most common configuration of the SAPF is a three phase three wire SAPF having single energy storage element. Applying Kirchhoff's voltage law at the junction point of SAPF with the grid leads to the equations in the "abc" frame as in the set of equations (1).

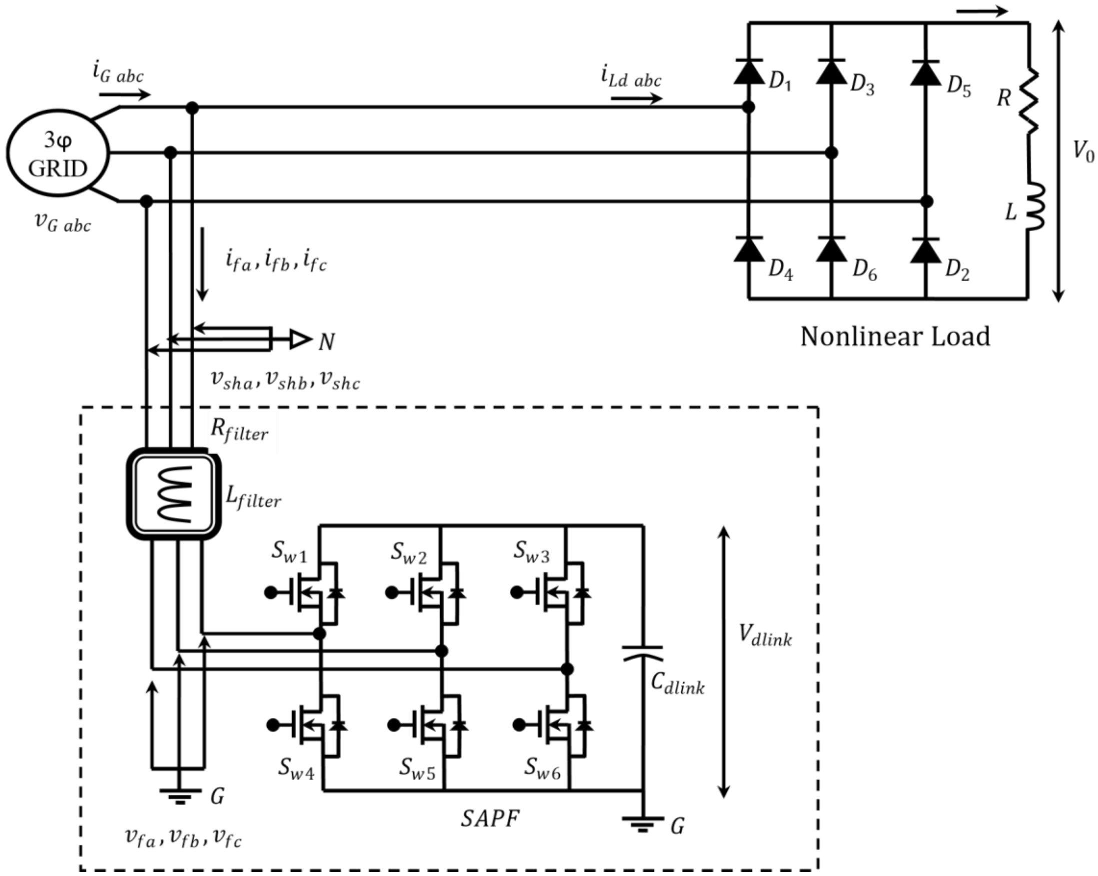

Fig 2.2 Circuit topology of three phase SAPF connected to the grid

$$v_{sha} = R_{filter} * i_{fa} + L_{filter} * \frac{di_{fa}}{dt} + v_{fa} + v_{GN} \quad ...1$$

Where, Vsha are the voltages measured between phase and neutral of the system after the filter inductor, v_{fa}, v_{fb} and v_{fc} are the voltages measured between the inverter output terminals and the ground point, v_{GN} is the voltage measured between ground to neutral, R_{filter} is the filter is the resistance and L_{filter} is the filter inductance. The neutral-to-phase APF voltages are given by the equation (2).

$$v_{fx} = v_{fa} + v_{GN}$$
$$v_{fy} = v_{fb} + v_{GN}$$
$$v_{fz} = v_{fc} + v_{GN} \quad ...2$$

3. Design of SAPF

The norms for designing SAPF taken here are, three phase VSI is used here to inject the essential current harmonics into the grid to compensate the grid current THD. Three phase grid voltages (v_{Ga}, v_{Gb} and v_{Gc}), three phase load currents(i_{La}, i_{Lb} and i_{Lc}), and three phase grid currents (i_{Ga}, i_{Gb} and i_{Gc}) are measured. Balanced three phase grid voltages with the supply frequency of 50 Hz is considered as shown in the equation (3).

$$v_{Ga}(t) = V_{mes} \cos(2\pi f_{mes} t) \quad \ldots 3$$

Where, V_{mes} and f_{mes} are the measured three phase grid voltages and the frequency, respectively.

- The sampling and switching frequency are chosen
- Pure inductance is considered for modelling

3.1. Design of DC Link Voltage

The grid voltage and frequency considered here for the three phase three wire system is 440 V, 50 Hz. The source resistance (R_{ser}) and inductance (L_{ser}) are considered as 0.04 Ω and 1mH, respectively. The DC link voltage design depends on the line voltage at PCC. The modulation index for this voltage is considered as unity. The output line voltage of the VSI is given by (V_{L-L}). The constraint for the selection of DC capacitor voltage is given as in equation (4).

$$V_{dlink} \approx \left(2\sqrt{(2/3)}\, V_{L-L}\right).Z \quad \ldots 4$$

V_{dlink} = DC link capacitor (C_{dlink}) voltage

V_{L-L} = Grid voltage (Line to Line)

Z = Modulation index

V_{dlink} must be almost equal to the peak value of the line voltage. Thus, V_{dlink} is selected as 700 V for (V_{L-L}) of 440 V and for a calculated V_{dlink} value of 718 V.

3.2. Design of DC Link Capacitor

The selection of DC link capacitor is based on the DC reference voltage and it is given by the equation (5). Here, ($V_{dlink-max}$) is the maximum value of the DC bus voltage, $i_{c(rated)}$ is the phase current of VSI, ω is the angular frequency and (t) is the recovery time of DC bus voltage.

$$\boldsymbol{C_{dlink} = \pi \times \frac{i_{c(rated)}}{\sqrt{3} \times \omega t \times V_{dlink-max}}} \quad \ldots (5)$$

where, ω =2π x50 = 314.159; $i_{c(rated)}$ = rated current, $V_{dlink-max}$= 700 V.

3.3. Design of Filter Inductor

The rating of filter inductance is calculated as per the equation (6).

$$L_{filter} = \frac{V_{dlink}}{2 \times (\Delta I_{rip-peak}) \times f_{sw-max}} \quad \ldots (6)$$

Where, (V_{dlink}) represents DC link voltage, (f_{sw-max}) represents maximum switching frequency, ($\Delta I_{rip-peak}$) represents peak to peak ripple current and their values are selected as V_{dlink} = 700 V, $\Delta I_{rip-peak}$ = 11.6 ,Amps, f_{sw-max} = 30,000 Hz = 30 kHz.

3.4. Rating of the Switching Devices

The power rating of the SAPF should be fixed first to select the voltage and current rating of the switching devices. The modelling is carried out in order to decide the perfect rating of the switching devices as follows.

$$Q_{switch} = V_{VSI}^2 / 2\pi f L_m \quad \ldots (7)$$

The reactive power flow (Q_{switch}) of VSI is depending on the magnetization inductance (L_m=0.0397H), frequency $(f = 50 \text{ Hz})$ and maximum line voltage of V_{VSI} (440 V). The VA rating of the voltage source inverter is obtained from the equation (8).

$$VA_{VSI} = \sqrt{P_{switch}^2 + Q_{switch}^2} \quad \ldots (8)$$

Where,(P_{switch}) represents active power flow and (Q_{switch}) represents the reactive power flow in VSI. From the calculation of apparent power rating and the inverter line voltage the current rating of the switch can be obtained as in equation (9).

$$I_{switch} = VA_{VSI} / (\sqrt{3} * V_{VSI}) \quad \ldots (9)$$

3.5. Reference Current and PWM Signal Generation

The current control algorithm has to be implemented with two main blocks, such as reference current generator and Space Vector Pulse Width Modulation (SVPWM) generator as shown in Figure 3.1

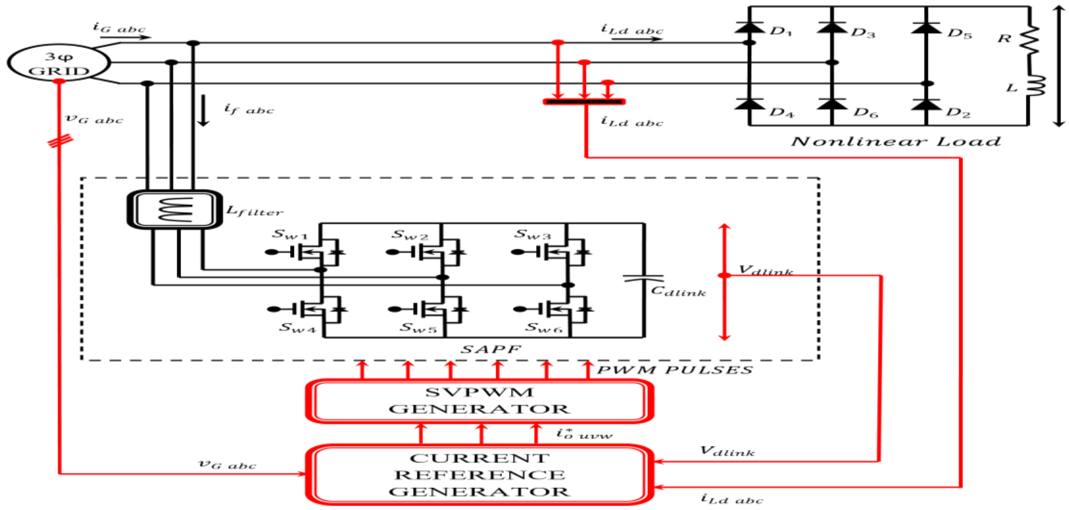

Fig 3.1 Reference current and PWM generation of SAPF

4. RESULTS AND DISCUSSIONS

The results obtained from the MATLAB simulation of SAPF to validate its performance in compensating harmonics and improving the power factor of the grid system. The harmonics are introduced in the grid by connecting a three phase Diode Bridge Rectifier (DBR) as nonlinear load. The DBR feeds supply to resistive and inductive load (R-L load). The simulated results discussed here assure that the designed SAPF performs well towards the objectives. The results are analyzed in two cases such as (i) Grid system with nonlinear load and (ii) Grid system with nonlinear unbalanced load. Table 3.1 gives the system parameters considered for simulation and Figure 4.1 and 4.2 shows a comparative THD value of with filter and without filter.

Table 4.1 System parameters for simulation

Name of the Parameters		Values
Grid voltage (v_G)		440 V, 50 Hz
Load power (P_{Ld})		2 kW
Filter inductor (L_{filter})		2.4 mH
DC link capacitor (C_{dlink})		1000 µF
Switching frequency		30 kHz
Nonlinear load	Three phase diode bridge rectifier	90 Ω, 130 mH
	Single phase diode bridge rectifier	300 Ω, 130 mH

Here, (v_G) represents the grid voltage, (i_G) represents the grid current, (i_{Ld}) represents the load current, and (i_F) represents the filter current (compensating current).

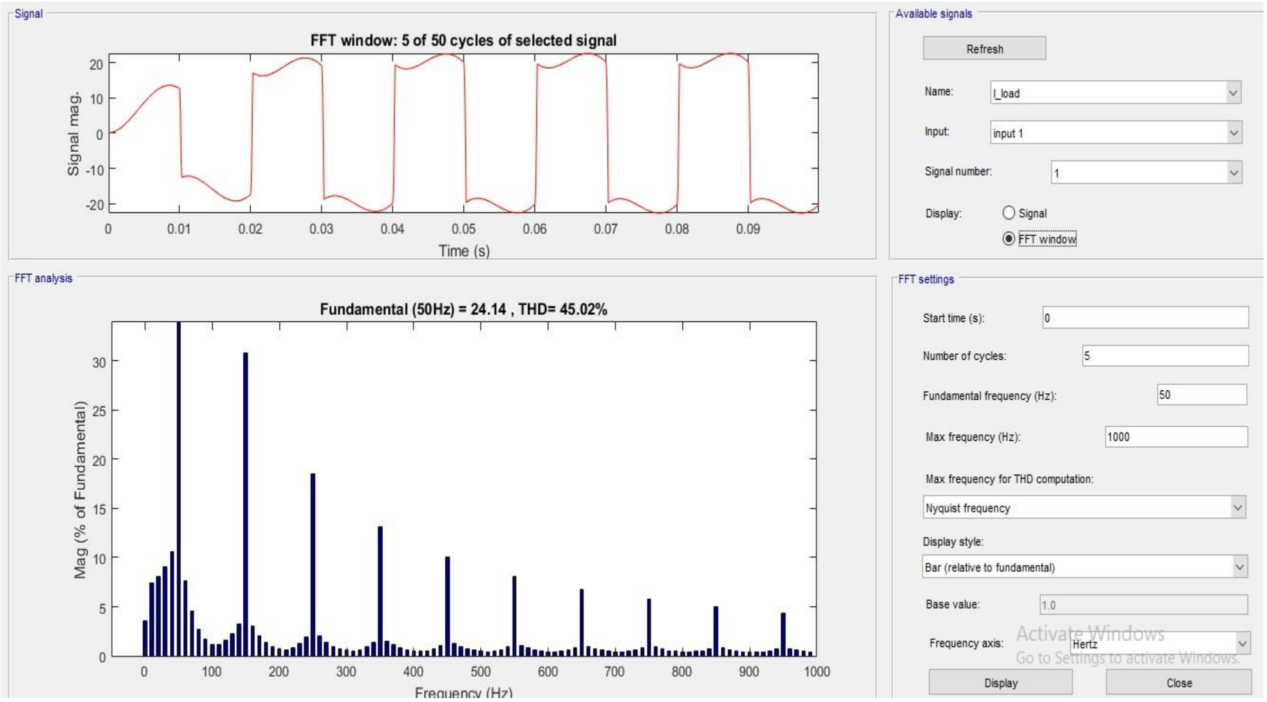

Fig 4.1 THD value without filter

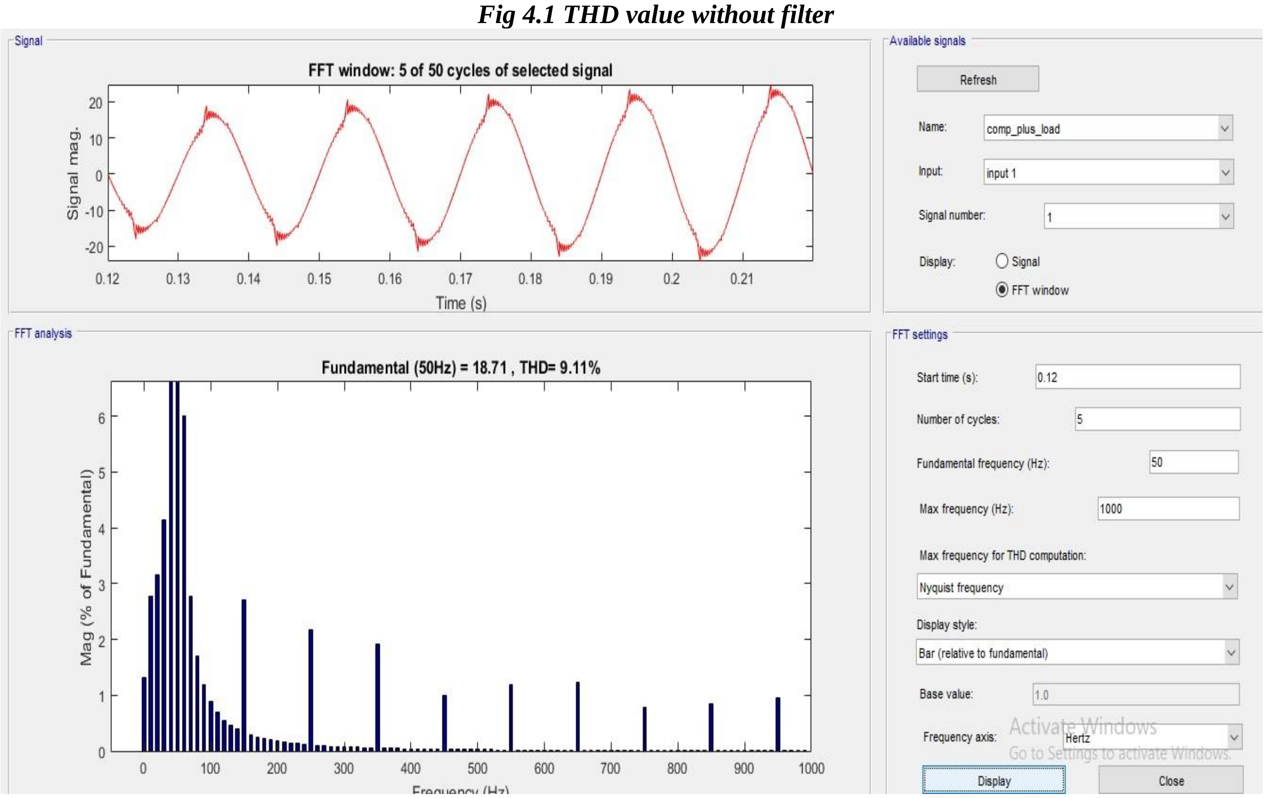

Fig 4.2 THD value with filter

5. CONCLUSION

It concludes the work carried out on the effective grid connected solar PV system with a two level converter performs as a parallel filter and an interfacing inverter with the modified CCMRF PLL with ICA based PI controllers. The simulations were carried out in MATLAB. The grid current THD from 45.02% to 9.11% and the power factor is improved from 0.92 to 0.992 under unbalanced voltage conditions of the grid.

- Under unbalanced current condition of the grid, the THD is reduced as 9.11% and the power factor is improved from 0.948 to 0.993.
- Under the balanced load condition, the THD of grid current is 3.28% and the power factor is improved from 0.942 to 0.995.
- The tracking, estimation/elimination of the grid synchronizing parameters such as voltage magnitude, theta and frequency tracking and elimination of DC component in the grid voltage were done with the better accuracy and speedy response by ICA tuned CCMRF PLL, compared to SRF PLL.

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Conflict of Interest

None of the authors have any conflicts of interest to declare.