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Beyond Synaptic Weight: Self-Adaptive Transistors and Memory Cells for Metaplastic Neuromorphic Hardware

Balaji Murugan [1, *]

[1] Department of Physics, Bannari Amman Institute of Technology, Sathyamanglam-638401, Tamil Nadu, India.
*Corresponding author Email: balaji@bitsathy.ac.in
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Abstract: Neuromorphic hardware has moved from CMOS spiking circuits toward resistive, phase-change, electrochemical, ferroelectric, low-dimensional, and optoelectronic devices in which memory and computation are physically coupled. However, most artificial synapses are still evaluated as first-order programmable elements: an input pulse changes conductance, and the resulting conductance is treated as the learned weight. This approach captures useful plasticity but does not fully represent the adaptive character of biological learning, where previous activity can alter the response to later stimulation. This mini-review examines self-adaptive neuromorphic transistors and memory cells from this higher-order perspective. A two-state framework is introduced in which W represents the observable synaptic weight and A represents a slower adaptive state that controls how W will respond to future inputs. Depending on the device platform, A may be associated with filament configuration, ion distribution, charge trapping, structural relaxation, ferroelectric domain statistics, reservoir chemistry, or a modulatory gate state. Resistive memories, phase-change devices, electrochemical memories and transistors, ferroelectric devices, two-dimensional memtransistors, and multimodal optoelectronic synapses are comparatively assessed for their ability to support such coupled states. Particular attention is given to metaplasticity, adaptive retention, consolidation, homeostatic regulation, heterosynaptic control, context-dependent learning, and continual learning. The review also proposes experimental criteria for separating genuine learning-rule adaptation from ordinary state-dependent switching, including matched-weight conditioning-probe tests, time-scale separation, recovery kinetics, cross-talk analysis, and system-level overhead. The central argument is that the next useful neuromorphic device should not only store what has been learned, but should also physically encode how subsequent learning should occur.

Keywords: Neuromorphic Computing, Artificial Synapse, Memristor, Synaptic Transistor, Adaptive Learning, In-Memory Computing

1. Introduction

Neuromorphic engineering was originally developed to implement neural computation with physical dynamics rather than reproduce the instruction-driven operation of conventional digital processors [1-4]. Large-scale platforms such as TrueNorth, SpiNNaker, and Loihi demonstrated the advantages of event-driven communication, distributed state, sparse activity, and local learning for brain-inspired workloads [5-9]. These CMOS systems established the architectural value of neuromorphic computing, but they also made clear that the cost of storing and moving synaptic parameters remains a major limitation when network size increases. The emergence of nonvolatile and partially volatile memory devices therefore shifted much of the field toward architectures in which memory and computation are colocated [10-16]. In resistive crossbars, for example, conductance can represent a weight while Kirchhoff's and Ohm's laws provide parallel multiply-accumulate operations, reducing repeated data movement between logic and memory [11, 12, 17-20]. This transition has been important because it changes the role of a memory element from passive storage to an active computational primitive. At the same time, it raises a more demanding question: whether a device can do more than store an analog weight and can instead participate directly in controlling the learning process itself.

The present device landscape is technically diverse, and each platform offers a different balance among density, update linearity, state retention, volatility, write energy, endurance, read-write separation, and controllability. Filamentary RRAM and memristors are attractive for compact two-terminal arrays and can provide rich history-dependent

dynamics, but stochastic filament formation, asymmetric updates, conductance-dependent programming sensitivity, and device-to-device variation complicate precise training [17, 18, 21-36]. Phase-change memory provides accumulative SET behavior, mature material physics, and compatibility with dense arrays, while conductance drift, stochastic crystallization, and the asymmetry between SET and RESET operations must be managed at the circuit and algorithm levels [37-46]. ECRAM and organic electrochemical transistors use ion-controlled channel doping and naturally separate the programming terminal from the read path, which can improve update symmetry and provide access to internal ionic variables, although ion transport, electrolyte stability, scaling, and process integration remain important challenges [47-58]. Ferroelectric devices offer field-driven polarization switching, nonvolatile state storage, and increasing compatibility with scaled CMOS processes, but analog operation depends on domain nucleation, domain-wall motion, interfacial trapping, imprint, and fatigue [59-66]. Multi-terminal 2D devices and optoelectronic synapses add strong gate or sensory control and can support context-dependent operation, but they currently face stronger constraints in contact engineering, wafer-scale uniformity, interfaces, packaging, and array-level reproducibility [67-77]. These differences mean that a single metric such as conductance-state count or energy per pulse is insufficient to identify the most useful platform for adaptive learning.

Most neuromorphic device papers describe plasticity through a familiar set of biological analogies, including excitatory postsynaptic current, paired-pulse facilitation, short-term plasticity, long-term potentiation and depression, spike-rate-dependent plasticity, and spike-timing-dependent plasticity [21, 22, 78-82]. These demonstrations are valuable because they show that physical state variables can respond continuously to temporal stimulation. However, many of these functions remain first-order in the engineering sense: once the present conductance and the applied pulse are known, the next conductance change follows a largely fixed update characteristic. Biological synapses operate with additional regulatory layers. Metaplasticity changes the ability of a synapse to undergo later plasticity, homeostatic mechanisms prevent uncontrolled excitation or depression, and consolidation allows selected traces to become more stable while less relevant information decays [80, 81, 83-85]. Therefore, two synapses with the same instantaneous efficacy can react differently to the same future stimulus if their previous activity histories have placed them in different internal adaptive states. This distinction is central for hardware intended for continual, nonstationary, or context-sensitive learning.

Evidence that device hardware can reproduce such higher-order behavior already exists, but it is distributed across material systems and is often described using different terminology. Memristive devices have demonstrated explicit synaptic metaplasticity in which conditioning modifies the magnitude or polarity of subsequent long-term plasticity [86, 87]. Other devices use a fast-to-slow transition to emulate consolidation, for example through charge-trap lifetime engineering, diffusive dynamics, or network relaxation [22, 25, 88, 89]. Astrocyte-inspired circuits and devices introduce negative feedback or resource regulation that can recover useful weight-update behavior and stabilize learning [90-92].

Heterosynaptic plasticity has been implemented by using additional terminals or internal trap populations so that one signal controls the plastic response associated with another pathway [67-70, 93]. Reconfigurable devices and neuromorphic systems have also begun to explore the transition between neuronal and synaptic functions or adaptation of learning parameters across tasks [94, 95]. Together, these results show that the physical substrate can contain more information than the externally measured conductance. The remaining problem is to define this extra state rigorously and determine when it provides a genuine computational advantage rather than another descriptive label for hysteresis. A representative experimental demonstration of this transition from conventional synaptic memory to adaptive neuromorphic hardware was reported by Bianchi et al., where resistive-switching synaptic arrays were coupled with additional internal-state memory elements to regulate neuronal excitability according to previous activity, reward, and penalty. The architecture illustrates how nonvolatile memory can be used not only to encode synaptic strength but also to retain an internal adaptive variable that modifies subsequent network response as shown in Figure 1(a-f) [96].

Figure 1 provides an important experimental example of how conventional synaptic memory can be extended toward history-dependent neuromorphic adaptation. In Figure 1a, the agent interacts with a dynamic environment through reward and penalty signals, while RRAM synapses determine the direction-dependent connection strength and an additional internal-state device regulates the neuronal firing threshold. Figure 1b summarizes the reinforcement-learning sequence, including initialization of the resistance matrices, neuronal integration, threshold comparison and iterative movement of the agent. The hardware organization is shown in Figure 1c, where separate synaptic and internal-state RRAM arrays are connected to an FPGA and a small number of CMOS neurons. Figure 1d illustrates the operation of an individual firing direction and shows that the internal RRAM state modifies the neuronal threshold independently of the primary synaptic connection.

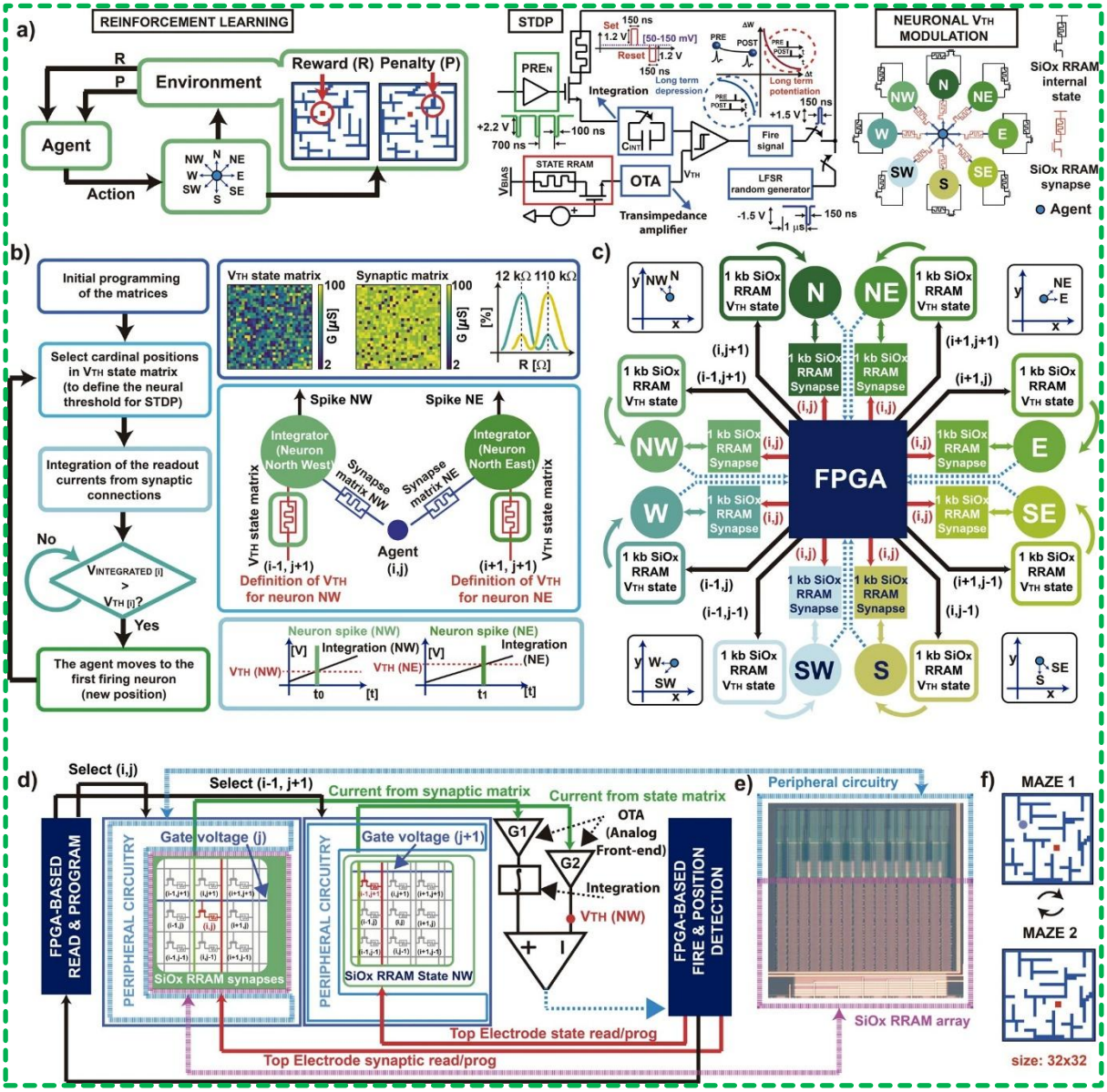

Figure 1 (a-f). Hardware implementation of experience-dependent self-adaptation using resistive-switching memory devices. The architecture combines synaptic RRAM arrays with additional internal-state RRAM elements that regulate neuronal excitability according to previous activity and reinforcement signals, providing a physical mechanism for history-dependent adaptation in neuromorphic hardware [96].

Figure 1e shows the physical memory array and peripheral addressing circuitry, demonstrating that the concept was implemented beyond simulation. Finally, Figure 1f introduces the dynamic-maze environment used to evaluate experience-dependent learning. From the perspective of the present review, the synaptic RRAM state can be associated with the fast functional weight W, whereas the threshold-controlling internal memory provides a practical example of an additional history-dependent adaptive variable related to A. This architecture therefore illustrates how a second physical state can regulate future network responses rather than merely storing another static weight [96]. To organize this problem, this review uses a minimal two-state description. The first state, W, is the variable directly interpreted as synaptic weight and is normally read as conductance, current, threshold, or optical transmission. The second state, A, is an adaptive variable that changes the future update law of W. A can be slower than W, partially hidden from ordinary readout, and may recover when conditioning is removed. In a filamentary memristor, W may be dominated by the effective conductive path while A reflects residual ion distribution, filament geometry, or interfacial chemical configuration [22, 25, 86, 87]. In PCM, W can be the effective phase-dependent conductance while A can reflect structural age, thermal history, subthreshold nuclei, or a coupled accumulator [37-45]. In ECRAM and OECT devices, the separated gate and channel offer a natural route for assigning W to channel conductance and A to ion-reservoir composition, interfacial state, or slow

chemical equilibration [47-56]. In ferroelectric devices, W may depend on the fraction of switched polarization while A arises from domain configuration, depolarization field, trapping, or another coupled ionic state [59-62, 97]. Multi-terminal and multimodal devices provide still more direct control because one gate or sensory input can modulate plasticity while another path stores the primary weight [67-77]. This W+A description is intentionally device-agnostic and is useful only when experiments can show that A changes the response to a later, otherwise identical learning stimulus.

This distinction also changes how device performance should be compared. Conventional analog-synapse metrics such as dynamic range, linearity, symmetry, state resolution, write noise, endurance, retention, energy, and variation remain essential [10-18, 23-27, 37-45, 47-56, 98]. For a self-adaptive device, however, an additional set of questions is required. Can two devices or two histories be prepared at the same W but different A? Does a standard probe pulse then produce different delta-W values? How large is the adaptive-update gain, how long does it persist, and can it be intentionally erased or reversed? Are W and A independently writable, or does changing A disturb the stored weight? What additional lines, sensing circuits, write-verify steps, or calibration procedures are required at array level? These questions are particularly important because ordinary nonlinearity, drift, hysteresis, or state-dependent switching can easily be misinterpreted as metaplasticity if matched-state controls are not used. A convincing experiment should therefore include conditioning-probe protocols, matched initial weights, recovery measurements, repeated-device statistics, and a physical model that connects the adaptive response to a measurable internal mechanism.

The motivation for this higher-order approach is practical rather than purely biomimetic. Continual learning systems must absorb new information without rapidly destroying previously useful representations; edge sensors must adapt to changing environmental statistics; analog arrays must remain usable despite drift and device variation; and local learning rules should ideally reduce rather than increase the need for expensive digital supervision. A slow adaptive state could reduce the learning rate of consolidated weights, increase plasticity when novelty is detected, regulate conductance away from saturation, tune retention according to repetition, or allow sensory context to gate electrical learning [83-95, 99]. The same idea may also help convert unavoidable physical memory, such as ionic redistribution or structural relaxation, into a computational resource. The scientific challenge is therefore not to maximize the number of biological functions demonstrated by one device, but to establish a causal and quantitatively useful relation between an internal history variable and a modified learning rule. This review examines that challenge across the main transistor and memory-cell platforms and uses it to identify the experimental benchmarks, integration strategies, and research directions needed for genuinely self-adaptive neuromorphic hardware.

1.1 Scope and Novelty of this Mini-Review

Broad reviews have already established the device physics and system opportunities of nonvolatile memories, in-memory computing, artificial synapses, ECRAM, ferroelectric devices, 2D synaptic transistors, organic neuromorphic electronics, multimodal sensing, and memristive neural networks [10-16, 19, 31, 45, 52-57, 60-63, 68, 69, 72, 98, 100]. The purpose of this mini-review is different. Rather than cataloguing every reported synaptic function or ranking materials by a single performance metric, it reorganizes the literature around the question of higher-order adaptation. The central criterion is whether a physical state exists that changes how a stored weight responds to future stimulation. This allows devices based on very different mechanisms to be compared using the same functional language.

Four requirements are used throughout the review. First, adaptive behavior should be distinguishable from ordinary conductance dependence by preparing matched W states with different histories. Second, the adaptive state should have a measurable time scale and recovery behavior that can be separated from the immediate weight update. Third, the proposed mechanism should be connected to a physical variable through electrical transients, microscopy, spectroscopy, modeling, or controlled perturbation where possible. Fourth, the additional adaptive function should be evaluated at circuit or algorithm level so that its benefit can be compared with the routing, sensing, calibration, and energy overhead required to access it. This framework is applied to RRAM and memristors, PCM, ECRAM/OECT, ferroelectric memories and transistors, 2D and multi-terminal devices, and optoelectronic or multimodal synapses, followed by discussion of metaplasticity, consolidation, homeostasis, continual learning, benchmarking, major engineering limitations, and future research directions.

2. Biological Design Principles Relevant to Adaptive Hardware

2.1 First-Order Plasticity is not Sufficient

Activity-dependent timing rules such as STDP established that the sign and magnitude of synaptic modification can depend on the relative timing of pre- and postsynaptic activity [78, 79, 82]. Short-term plasticity adds another layer because synaptic response depends on recent activity over milliseconds

to seconds, while long-term processes persist over far longer times [80, 81]. Electronic devices have successfully reproduced many of these phenomena, but the key engineering distinction is whether history merely changes W or changes the mapping from stimulus to ΔW.

2.2 Metaplasticity, Homeostasis and Consolidation

Metaplasticity was defined as the plasticity of synaptic plasticity: activity can change the ability of a synapse to undergo subsequent potentiation or depression without necessarily producing an immediate change in baseline efficacy [83]. Homeostatic plasticity addresses a complementary stability problem, using negative feedback to keep neuronal activity within a functional range despite ongoing Hebbian changes [84, 85]. Consolidation stabilizes selected traces so that frequently or meaningfully reinforced information survives whereas weak or unused traces decay. For electronics, these mechanisms map naturally to three engineering functions: adaptive programming gain, global/local stabilization, and history-dependent retention [86-94, 99].

2.3 A Minimal W+A Model for Device-Level Metaplasticity

It is proposed that a minimal abstraction in which the read weight W and an adaptive state A obey different time scales. In a continuous description, $dW/dt = F[u(t),W,A]$ and $dA/dt = \varepsilon G[u(t),W,A]$, with $\varepsilon << 1$ for a slower adaptive variable. A may represent filament morphology, distributed trap occupancy, ion concentration in a reservoir, ferroelectric domain configuration, interfacial redox state, or an explicitly coupled second device. The key observable is not A itself but its effect on a standardized probe: ΔWprobe(A). A device should therefore be called metaplastic only when conditioning changes ΔWprobe in a reproducible way after accounting for the initial W. This criterion is stricter than demonstrating different conductance trajectories under different pulse trains and can prevent over-interpretation of ordinary nonlinear switching as higher-order learning [83, 86, 87, 99]. A hardware-oriented implementation of metaplasticity has been demonstrated by introducing an additional variable that regulates the probability of subsequent synaptic modification. Such approaches provide an important link between the conventional conductance state of a memristive synapse and a slower variable controlling the stability-plasticity balance during continual learning (Figure 2(a-c)) [101].

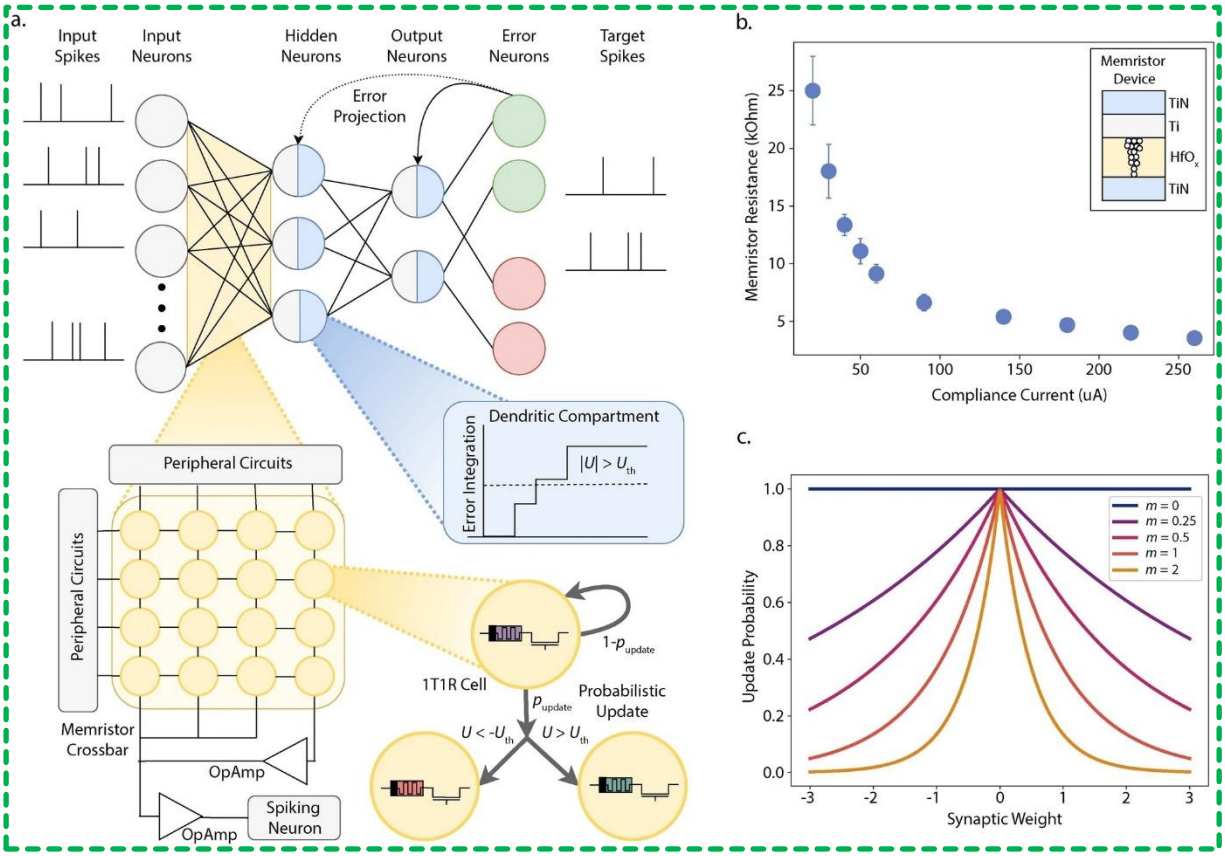

Figure 2 (a-c). Probabilistic metaplasticity implemented with low-precision memristive synapses for continual learning. The framework combines 1T1R memristive synaptic weights with a metaplastic mechanism that modifies the probability of subsequent weight updates according to weight state and previous activity, thereby regulating the balance between plasticity and stability [101].

Figure 2 illustrates how metaplasticity can be introduced into low-precision memristive learning without requiring continuously precise weight updates. Figure 2a presents a spiking neural network in which synaptic weights are implemented using 1T1R memristive crossbars. Errors are accumulated in dendritic compartments, and a weight becomes eligible for modification when the local error reaches a threshold. Importantly, eligibility alone does not guarantee programming; the update is additionally controlled by a probability that depends on the metaplastic state. Figure 2b shows experimentally derived resistance levels of the memristor as a function of programming compliance current, emphasizing that practical devices provide only a limited number of distinguishable states rather than ideal continuous weights. Figure 2c then presents the essential metaplastic mechanism: the probability of updating a weight decreases as either the magnitude of the synaptic weight or the metaplasticity coefficient increases. Consequently, frequently used or important connections progressively become more resistant to modification. Within the W+A description proposed in this review, the programmed memristor conductance corresponds to W, whereas the metaplasticity coefficient plays a role analogous to A by controlling the probability that W will change during a subsequent learning event. This provides a clear computational example of plasticity-of-plasticity and directly addresses the stability-plasticity problem in continual learning [101].

3. Device platforms: what can physically carry W and A?

3.1 Two-terminal RRAM and memristors

Two-terminal memristive devices remain attractive because they combine high density, analog conductance states and direct crossbar compatibility [10, 11, 15-27, 29-36,100]. Early work established STDP-like updates and multilevel tuning [21, 23], while Ag2S atomic switches showed a frequency-dependent transition from volatile short-term behavior to persistent conductance [22]. Diffusive memristors made this separation especially explicit: mobile species can relax spontaneously at one stimulation regime yet form more stable conductive structures under repeated excitation [25]. Such devices naturally suggest W+A implementations in which filament conductance serves as W while a slower structural variable-cluster distribution, reservoir depletion, interface chemistry or trap population-sets the probability or magnitude of subsequent switching.

The limitation is identifiability. A two-terminal I-V response often collapses multiple internal degrees of freedom into one measured conductance. The same conductance can arise from different microscopic configurations, which is useful for hidden-state computing but difficult for deterministic training. Device-to-device variability, abrupt filamentary events, asymmetric potentiation/depression and state-dependent update size remain major algorithmic concerns [17, 18, 23-28]. Multi-memristive synapses, write-and-verify schemes, and algorithm-aware training can compensate these nonidealities [18, 23, 26, 27], but compensation is not equivalent to intrinsic self-adaptation. The strongest evidence for device-level metaplasticity comes from conditioning experiments where the same probe stimulus produces a different update after a prior activity history [86, 87, 99].

3.2 Phase-Change Memory: Useful Separation between Accumulation, Drift and Stochasticity

Phase-change memory (PCM) stores state through the amorphous/crystalline configuration of chalcogenide material. Partial SET operations provide accumulative analog programming, whereas RESET is generally more abrupt; conductance drift and stochastic nucleation add additional state dependence [37-46]. PCM has supported large synaptic arrays [38], stochastic neurons [39], temporal-correlation detection [40], mixed-precision computation [41], and photonic in-memory architectures [42-44]. These demonstrations show an important lesson for adaptive hardware: a nonideality such as stochasticity or relaxation can become a computational resource when the algorithm explicitly models it.

For W+A operation, PCM offers several candidate separations. W can be represented by effective conductance or optical transmission, while A may be associated with structural age, temperature history, projected-device substate, or an auxiliary volatile accumulator. However, drift that simply perturbs W is not automatically metaplastic. A convincing adaptive demonstration would condition the phase configuration or thermal history, return the device to a matched W, and then show a systematically modified SET/RESET response. PCM is therefore an excellent platform for studying whether physically distinct but coupled structural descriptors can be exposed as a controllable second learning variable [37-45].

3.3 ECRAM and organic Electrochemical Transistors: Clean Read/Write Separation and Ionic State Variables

Electrochemical transistors are particularly well matched to the W+A concept because the gate drives ionic redistribution while a separate source-drain path reads electronic conductance [47-58, 98]. PEDOT:PSS OECTs first established rich short-term neuromorphic dynamics [47], while Li-ion synaptic transistors and nonvolatile organic electrochemical

devices demonstrated gradual low-voltage conductance modulation [48, 49]. More recent protonic devices operate on nanosecond time scales [51], and integrated ECRAM arrays show linear, symmetric open-loop programming that is highly desirable for analog learning [54]. Reviews of the field emphasize the importance of ion species, electrolyte/channel interfaces, and redox thermodynamics in determining speed, retention and symmetry [52, 53, 55, 56].

Figure 3 demonstrates the device-to-array progression of an electrochemical random-access memory platform and highlights several features that make ECRAM attractive for adaptive neuromorphic hardware. Figure 3a shows the fabricated 10 x 10 array, establishing the scalability of the concept beyond an isolated device. The cross-sectional TEM image in Figure 3b identifies the W/YSZ/WOx stack, in which the WOx layer functions as the conductance-modulated channel and the YSZ layer provides the ionic transport pathway. Figure 3c demonstrates approximately linear and symmetric conductance modulation during repeated potentiating and depressing pulse sequences, a particularly valuable characteristic for analog training because it reduces state-dependent update errors. Figure 3d contrasts open-loop programming with conventional closed-loop write-and-verify operation. Because conductance change can be predicted from pulse number, the open-loop approach reduces the need for repeated sensing and feedback. Figure 3e demonstrates array-level programming of multiple image patterns and confirms the practical controllability of the conductance states. In the present W+A framework, this experiment primarily demonstrates accurate control of W rather than metaplasticity itself. Nevertheless, the separated ionic gate and electronic read path provide a promising physical basis for introducing a second slower reservoir, interfacial or chemical variable that could subsequently function as A [54].

The most direct self-adaptive architecture would use at least two ionic reservoirs or two kinetic pathways. A fast ion population could modulate channel conductance (W), whereas a slower reservoir composition, interfacial chemical state or polymer morphology could set the ease with which subsequent ions enter/leave the channel (A). This is conceptually similar to short-term facilitation superimposed on a slower homeostatic variable. The three-terminal geometry also enables a modulatory terminal that changes plasticity without disturbing readout. The cost is materials/process complexity: electrolyte encapsulation, retention-speed tradeoffs, environmental sensitivity and back-end-of-line compatibility can become more difficult than in solid-state two-terminal memories [47-56, 98].

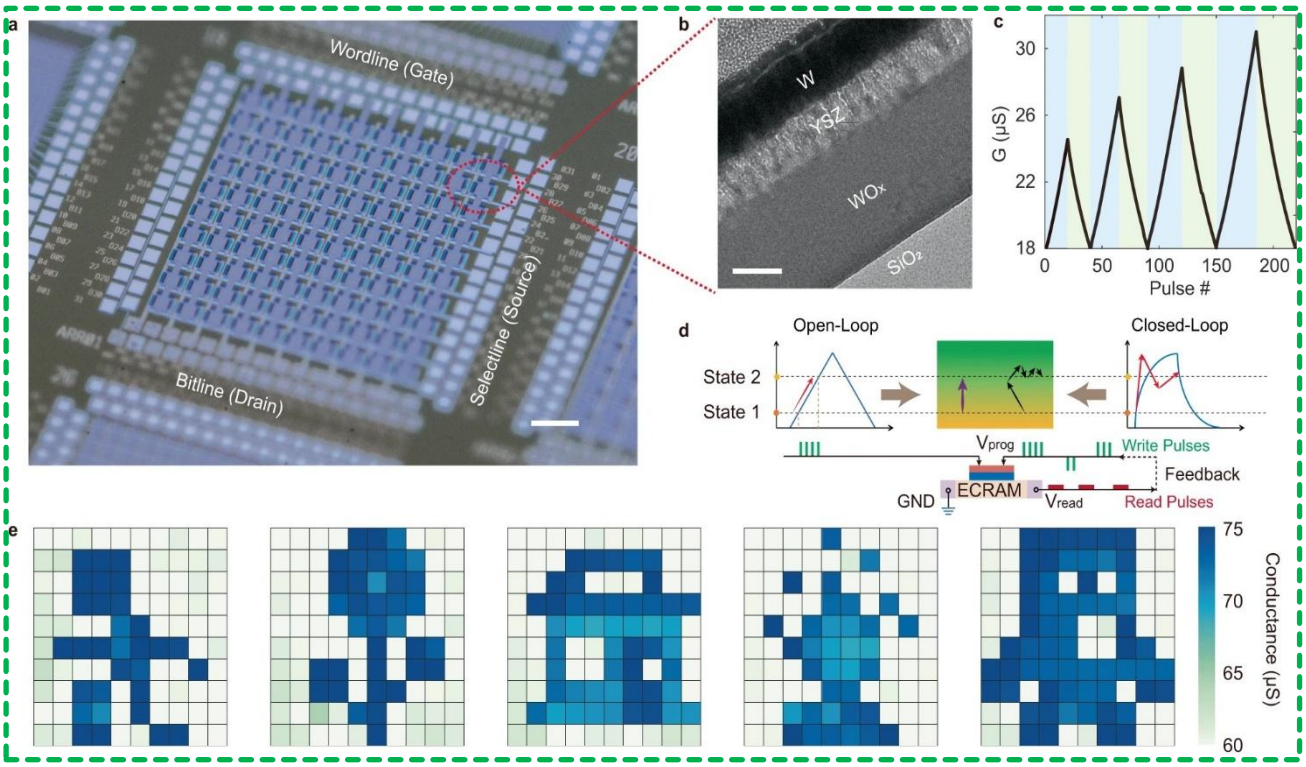

Figure 3 (a-e). Electrochemical random-access memory array exhibiting linear and symmetric analog conductance programming. The figure shows the integrated ECRAM array, W/YSZ/WO_x device structure, pulse-dependent conductance modulation, open-loop programming strategy, and array-level image programming [54].

3.4 Ferroelectric Memories and Transistors: Domain Statistics as an Adaptive State

Ferroelectric synapses encode history through polarization and domain switching. Domain-wall dynamics can produce gradual conductance evolution [59], while polymer and HfO_2-family FeFET/FTJ structures offer nonvolatile states, low-voltage operation and increasing CMOS relevance [60-66]. Compared with filamentary RRAM, ferroelectric switching provides a physically interpretable collective state: the fraction and spatial distribution of switched domains. Yet the same macroscopic polarization may correspond to different domain microstructures, creating an opportunity for hidden adaptive states if the microstructure affects later nucleation and switching. Figure 4 provides microscopic evidence for the physical origin of gradual conductance modulation in ferroelectric synapses. Figure 4a shows that repeated electrical pulses do not switch the ferroelectric layer uniformly; instead, multiple reversed domains nucleate progressively while domain propagation remains spatially limited. Figure 4b demonstrates that the fraction of switched ferroelectric area evolves systematically with cumulative stimulation and is accompanied by a corresponding change in junction conductance. This relationship establishes a direct connection between microscopic domain configuration and the electrical synaptic weight. Figure 4c further shows that switching kinetics are strongly dependent on pulse amplitude, indicating that the internal domain population retains information about both stimulation time and field strength. These observations are particularly relevant to the W+A framework. The macroscopic conductance can serve as W, whereas the spatial domain distribution, nucleation density or residual unswitched regions may contain additional history information that influences later polarization switching. However, domain configuration should only be identified as A if different domain histories prepared at comparable W values produce distinguishable responses to the same subsequent probe pulse. Thus, ferroelectric domain imaging provides an experimentally accessible route for testing whether microscopic state degeneracy can be converted into useful adaptive plasticity [59].

A particularly relevant direction is to deliberately couple ferroelectric polarization to a second process. The 2026 ferroelectric-ionic-trapping transistor combines polarization, oxygen-vacancy migration and charge trapping in one device [97].

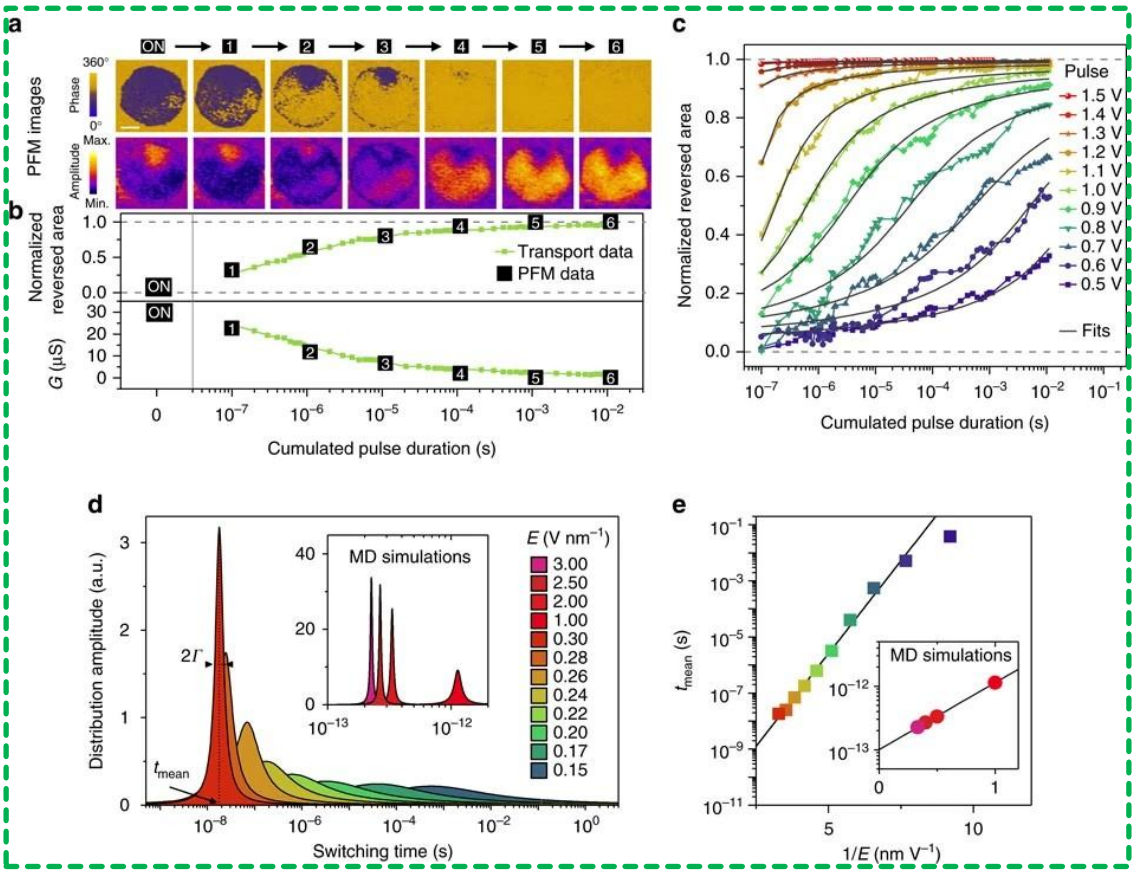

Figure 4 (a-c). Ferroelectric domain dynamics underlying gradual synaptic conductance modulation. **(a)** Piezoresponse-force microscopy phase and amplitude images showing progressive domain nucleation under cumulative voltage pulses. **(b)** Evolution of normalized switched ferroelectric area and corresponding device conductance as a function of accumulated pulse duration. **(c)** Dependence of the switched-area evolution on programming voltage amplitude [59].

Such coupled physics can in principle assign W to one state variable and A to another, but only if experiments decouple their roles. The field should therefore move from demonstrating more synaptic functions in a single transfer curve to perturbation experiments that isolate which physical variable controls retention, threshold, update gain and recovery. Reliability issues-imprint, fatigue, depolarization, trap-assisted drift and device-to-device domain statistics-must be reported as both limitations and potential adaptive degrees of freedom [59-66, 97].

3.5 2D Memtransistors and Multi-Terminal Synaptic Transistors

Two-dimensional materials are attractive for adaptive neuromorphic transistors because atomically thin channels are strongly coupled to gates, interfaces, adsorbates and ferroelectric layers. Multi-terminal MoS_2 memtransistors demonstrated gate-tunable memory and heterosynaptic functionality [67], while electrolyte-gated MoS2 devices used multiple gates to emulate gain modulation and higher-order neuronal functions [70]. Recent reviews catalog a wide variety of three-terminal 2D synapses based on charge trapping, ion motion, ferroelectric coupling and floating gates [68, 69]. The architectural advantage is clear: one terminal can program W and another can modulate A, enabling direct experimental tests of heterosynaptic or context-dependent plasticity. Three-terminal synaptic transistors provide additional physical degrees of freedom compared with conventional two-terminal memories because weight storage, signal transmission, and modulatory control can be partially separated through different terminals and functional layers. This architecture (Figure 5(a-c)) is particularly attractive for implementing a primary synaptic state together with an independently addressable adaptive or contextual variable [68]. Figure 5 compares three representative three-terminal device architectures that provide greater physical separation between memory programming, signal transmission and modulatory control than conventional two-terminal memories. Figure 5a illustrates a floating-gate field-effect transistor in which charge stored in an electrically isolated floating gate shifts the channel threshold and therefore controls the synaptic conductance. The tunneling and blocking layers determine charge injection, retention and erase dynamics. Figure 5b shows a ferroelectric field-effect transistor, where the polarization state of the ferroelectric gate dielectric controls channel conductivity and provides nonvolatile weight storage.

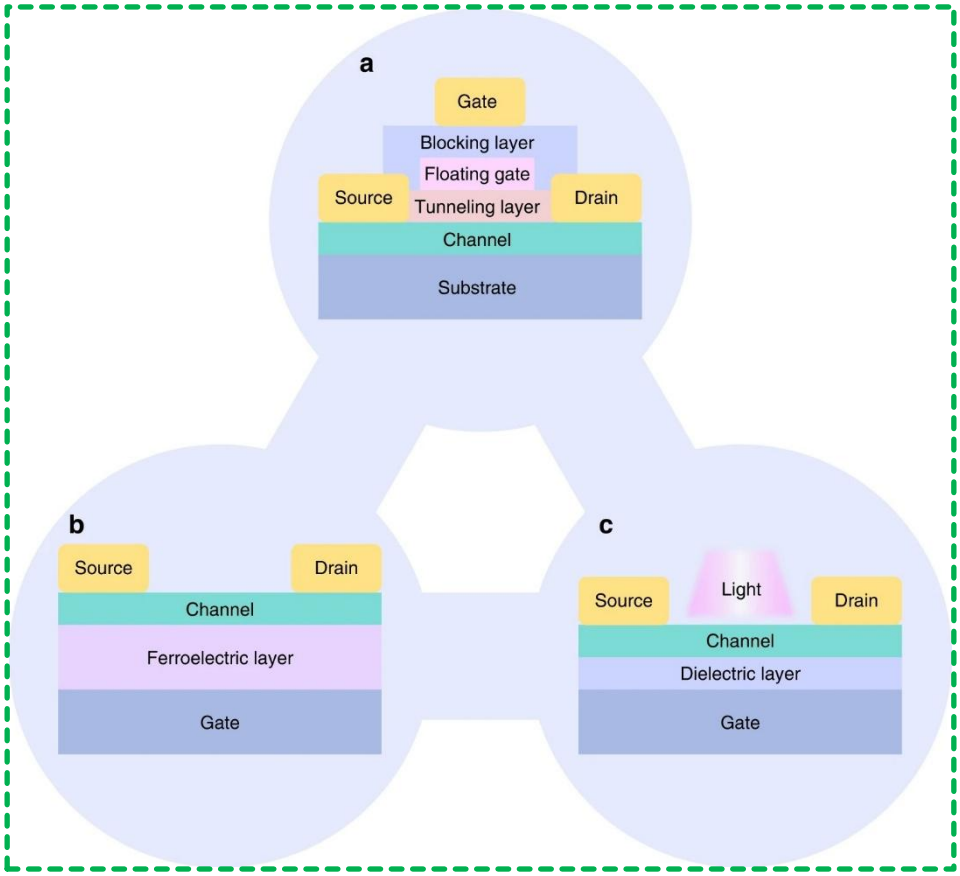

Figure 5 (a-c). Representative structures of three-terminal artificial synaptic transistors, including floating-gate, ferroelectric, and optoelectronic field-effect transistor configurations. The additional control terminal provides an architectural route for separating synaptic weight modulation from contextual or adaptive control [68].

Figure 5c represents an optoelectronic field-effect transistor in which optical stimulation acts in addition to electrical gate control, introducing an extra sensory degree of freedom. These structures demonstrate why multi-terminal devices are particularly relevant to self-adaptive neuromorphic hardware: the primary channel conductance can represent W, while a gate, trapped-charge population, polarization configuration or optical control variable may independently influence the subsequent update response. However, the structures shown in Figure 5 are architectural examples rather than direct demonstrations of metaplasticity. Their principal advantage is therefore the availability of orthogonal control terminals that could be exploited experimentally to separate W and A and quantify cross-talk between the two states [68].

The weakness is manufacturability. Contact resistance, defect density, interfacial contamination, transfer variability and wafer-scale uniformity can dominate apparent synaptic behavior. Thus, a high-functionality single-device demonstration should not be treated as evidence of array viability. For self-adaptive hardware, the most compelling 2D route is not to maximize the number of behaviors but to exploit orthogonal control knobs-for example gate-controlled trap occupancy plus channel conductance, or ferroelectric polarization plus photocarrier trapping-while quantifying cross-talk and cycle stability [67-70, 75-77].

3.6 Optoelectronic and Multimodal Synapses: Context as A Physical Input

Neuromorphic sensing creates a natural role for A because different sensory modalities can modulate the learning response to the same electrical event. Multimodal reviews now cover visual, tactile, chemical, auditory and other input channels [72]. GaN photoelectrochemical synapses combine photo-electric and chemical-electric processes [73], molecularly engineered memristors can retain wavelength-dependent photodipole states [74], and recent ferroelectric/2D devices couple polarization, anisotropic photodetection and memory [75-77]. Such devices blur the boundary between sensing, memory and modulation: an optical or chemical context signal can set A while electrical conductance remains W.

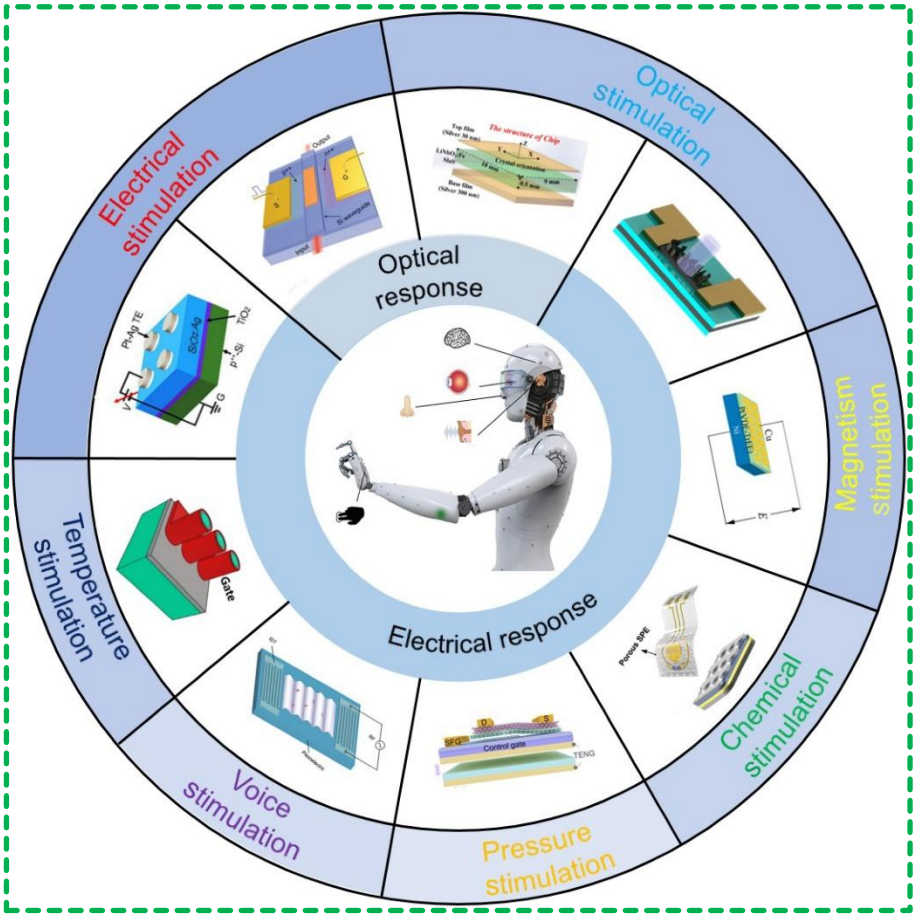

Figure 6. Classification of multimodal artificial synapses according to their stimulation and response modalities. Multimodal synaptic devices enable sensory information to be directly coupled with memory and neuromorphic processing, providing potential hardware pathways for context-dependent and multisensory learning [72].

Multimodal artificial synapses extend neuromorphic hardware beyond purely electrical stimulation by allowing optical, mechanical, chemical, thermal, acoustic, and other environmental signals to participate directly in synaptic modulation. These additional input dimensions provide a potential physical route for context-dependent adaptation when the contextual stimulus changes the subsequent learning response rather than only the instantaneous output [72].

Figure 6 broadens the concept of synaptic modulation from purely electrical programming to multimodal sensory interaction. The classification includes electrical, optical, magnetic, chemical, pressure, acoustic and temperature stimulation, reflecting the wide range of environmental signals that can potentially modulate an artificial synapse. Most reported devices ultimately convert these stimuli into an electrical response, while optically responding synapses provide an additional output modality. This organization is important for self-adaptive systems because different modalities need not play equivalent roles. One stimulus can provide the primary information used to update W, whereas another modality can act as a contextual or modulatory input that changes the susceptibility of the device to later learning. For example, optical exposure could modify trap occupancy or polarization, chemical stimulation could alter an ionic reservoir, and pressure or temperature could temporarily modify transport kinetics. Such effects become relevant to the A state only when they persist sufficiently to modify a subsequent learning event after the original contextual stimulus has been removed. Therefore, Figure 6 should be interpreted as a map of possible physical inputs for adaptive control rather than direct proof of metaplasticity. Table 1 summarizes the candidate weight (W) and adaptive (A) states, key advantages, and principal engineering limitations across the device platforms discussed in this section.

Table 1. Comparative platform assessment for self-adaptive neuromorphic cells

Platform	Terminals	Candidate W	Candidate A	Strength	Main barrier	Refs
RRAM / memristor	2	filament/interface conductance	filament morphology, mobile-species reservoir, trap population	very high density; crossbar compatible	hidden-state ambiguity; nonlinear/ asymmetric update	[17, 18, 21-28, 86, 87]
PCM	2	crystal/ amorphous fraction	structural age, thermal history, volatile accumulator	fast; mature arrays; stochastic dynamics	drift; RESET asymmetry; heating	[37-45]
ECRAM / OECT	3+	electrochemical channel doping	reservoir composition, interfacial redox state, slow ion population	decoupled read/write; linear analog update	electrolyte integration; retention-speed tradeoff	[47-57, 98]
FeFET / FTJ	2-3	polarization/ domain state	domain distribution, trapping, ionic state	nonvolatile ; HfO_2 CMOS path; low-voltage gating	fatigue/imprint ; domain variability	[59-66, 97]
2D memtransistor	3+	channel conductance / trapped charge	modulatory gate, interface state, ferroelectric coupling	heterosynaptic control; strong electrostatics	contacts, defects, wafer uniformity	[67-70]
Opto-/multimodal	2-3+	electrical weight / persistent photo conductance	spectral, chemical or polarization context	sensor-memory-learning fusion	calibration; environmental stability	[72-77]

The important experimental distinction is between multimodal sensing, where the instantaneous output changes, and context-dependent plasticity, where the future learning rule itself is altered [72]. This is highly relevant to edge intelligence, but evaluation must distinguish adaptive learning from sensor hysteresis. A useful protocol is to set identical W values under different contextual histories, then apply the same training sequence and compare the update trajectory. If context changes only the measured current during illumination, it is sensing modulation; if it changes subsequent plasticity after the context signal is removed, it is closer to metaplasticity. This distinction should become standard in claims of multimodal neuromorphic cognition [72-77].

4. From plasticity to adaptive plasticity: functions that should define the next device generation

4.1 Metaplasticity: conditioning the learning response

Memristive metaplasticity has already been demonstrated explicitly. Wu et al. reproduced history-dependent shifts in subsequent plasticity across several memristor types [86], and $KNbO_3$ devices showed both synaptic plasticity and metaplasticity under controlled spike histories [87]. More recent nanoparticle-engineered devices combine metaplasticity with reservoir computing [99]. These studies establish that higher-order plasticity is physically plausible, but they also reveal the need for stronger benchmarking: matched starting conductance, standardized probe pulses, conditioning dose-response curves, recovery kinetics, cycle-to-cycle reproducibility and separation from ordinary state-dependent switching.

4.2 Consolidation and Adaptive Forgetting

Biological memory is not optimized for indefinite retention of every event. Hardware likewise benefits from selective stabilization. An InP FET artificial synapse used charge-trap lifetime engineering to emulate transition from short-term to long-term memory [88], while nanowire networks showed sleep-dependent consolidation-like behavior [89]. Diffusive memristors and ionic devices also provide natural volatile-to-nonvolatile transitions [22, 25, 47-51]. The device-design goal should therefore be tunable retention rather than maximal retention: weakly relevant information should decay cheaply, whereas repeated or rewarded patterns should recruit a slower state that stabilizes W. History-dependent retention provides an experimentally accessible route from first-order plasticity toward memory consolidation. Repeated stimulation can progressively suppress relaxation and stabilize the synaptic state, indicating that retention itself can evolve according to previous training rather than remaining a fixed material parameter [102]. Figure 7 provides a clear experimental demonstration that memory retention in a memristive synapse depends on previous stimulation history. Figures 7a-e show the normalized synaptic-weight decay after training with N = 10, 30, 60, 90 and 120 pulses, respectively. At low pulse number, the synaptic weight decays rapidly after stimulation, indicating that a large fraction of the induced state is volatile and therefore resembles short-term plasticity.

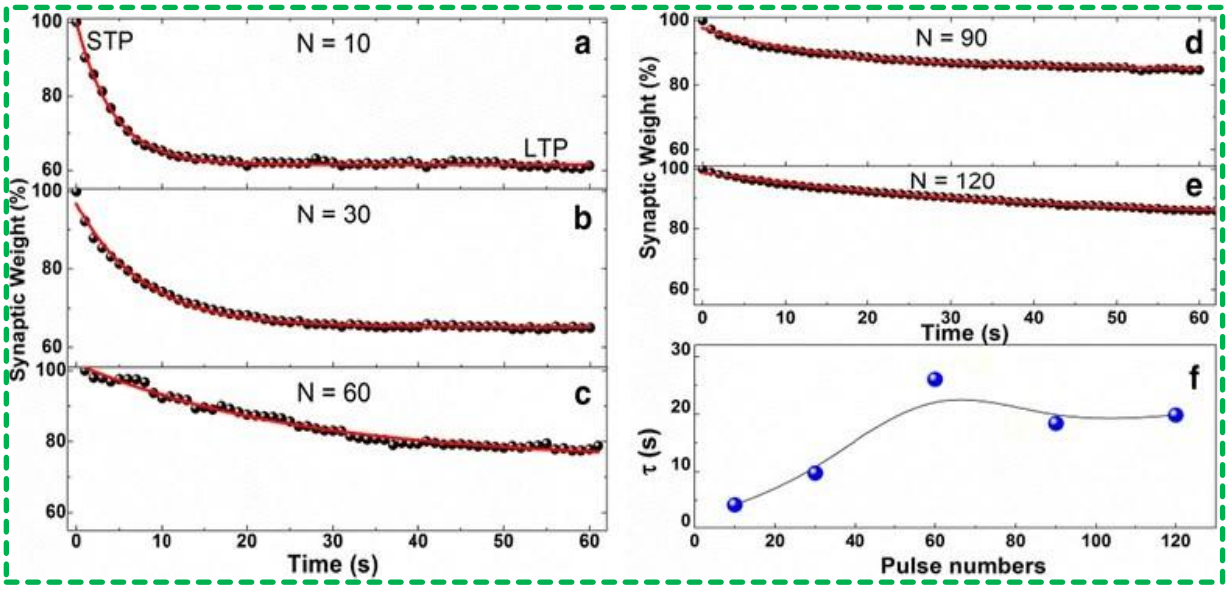

Figure 7 (a-f). Transformation from short-term plasticity to long-term plasticity in a Pt/HfOx/ZnOx/TiN memristive synapse under repetitive pulse stimulation. The retention curves demonstrate progressively reduced forgetting with increasing pulse number, while the extracted relaxation time increases with training, illustrating activity-dependent stabilization of the synaptic state [102].

Increasing the number of training pulses progressively reduces the decay rate and increases the residual long-lived component. At N = 90 and 120, the retention becomes substantially more stable, indicating a transition toward long-term plasticity. The authors report that the forgetting fraction decreases from approximately 40% to about 15% as training is increased, with the response tending toward saturation at high pulse number.

Figure 7f quantifies this evolution through the fitted relaxation time, which increases with stimulation history. This behavior is highly relevant to adaptive retention because the effective memory lifetime is not fixed but depends on the previous training dose. In the W+A interpretation, the measured synaptic conductance is W, while a slower structural, ionic or trap-related configuration induced by repeated stimulation could be viewed as a candidate adaptive state influencing the persistence of W. Importantly, this experiment demonstrates history-dependent consolidation, although additional matched-W conditioning experiments would still be required to establish fully independent device-level metaplasticity [102].

4.3 Homeostasis and Astrocyte-Inspired Regulation

Pure Hebbian learning is unstable because positive feedback can drive weights toward saturation; biological circuits counter this through homeostatic and glial regulation [84, 85]. Hardware work is beginning to address this limitation. Artificial astrocyte memristors have been used to recover weight-update linearity [90], a tripartite transistor architecture has been proposed for homeostatic control [91], and a biomimetic astrocyte-memristor system has demonstrated resource-aware stabilization [92]. These approaches shift the design objective from reproducing a single synaptic waveform to regulating the operating range of a network. For practical arrays, the central question is whether homeostatic control can be local and physically cheap enough to avoid replacing a device-level advantage with peripheral circuitry overhead.

Figure 8 shows how a separate internal memory state can provide activity-dependent homeostatic control during reinforcement learning. Figures 8a-e describe the stepwise navigation operation: the FPGA identifies the present location, stimulates the relevant synaptic devices, detects neuronal firing, updates the corresponding synaptic connection and then modifies the internal-state device associated with the newly visited location. Figure 8f demonstrates that repeated visits progressively increase the neuronal threshold, thereby reducing the probability of repeatedly selecting the same state and promoting further exploration.

Figures 8g and 8h show that this internal threshold is additionally modified by environmental feedback: penalties increase the threshold, whereas rewards decrease it and therefore increase the probability of revisiting favorable trajectories. Figure 8i illustrates saturation of the internal-state resistance, which introduces a physical boundary to the homeostatic response. Figures 8j and 8k show simultaneous potentiation/depression of the primary synaptic connections, while Figure 8l demonstrates that previous reward history influences adaptation when the environment subsequently changes. The figure therefore separates conventional synaptic plasticity from a slower regulatory state controlling neuronal excitability. In the terminology of this review, the synaptic connection represents W, whereas the history-dependent threshold memory provides a particularly clear physical realization of an A-like variable [96].

4.4 Heterosynaptic plasticity and modulatory terminals

Heterosynaptic plasticity means that activity at one pathway influences plasticity at another. Multi-terminal devices are a natural electronic analogue because a gate can modulate a channel without serving as the primary weight-update path [67-70]. Notably, heterosynaptic behavior has also been implemented in a vertical two-terminal device by exploiting internal trap modulation [93], indicating that extra functional dimensions do not always require extra external terminals. The engineering trade-off is therefore between external controllability and density: more terminals make A observable and programmable, whereas hidden internal states improve density but complicate calibration.

4.5 Reconfigurable Neuron-Synapse Operation and Learning-To-Learn

A further step is to reconfigure the computational role of the device itself. A steep-switching nonvolatile transistor has demonstrated reconfigurable neuron and synapse operation [95]. At the system level, neuromorphic hardware has also implemented learning-to-learn using plasticity parameters that adapt over tasks [94]. These results point toward a hierarchy: adaptive devices modify their update rule; adaptive circuits modify local learning parameters; meta-learning systems modify how those parameters are selected across tasks. Device-level W+A dynamics could provide a physical substrate for such meta-learning if A can be exposed to the algorithm without expensive readout. Table 2 consolidates these higher-order adaptive functions, their minimum experimental evidence, and representative physical implementation mechanisms.

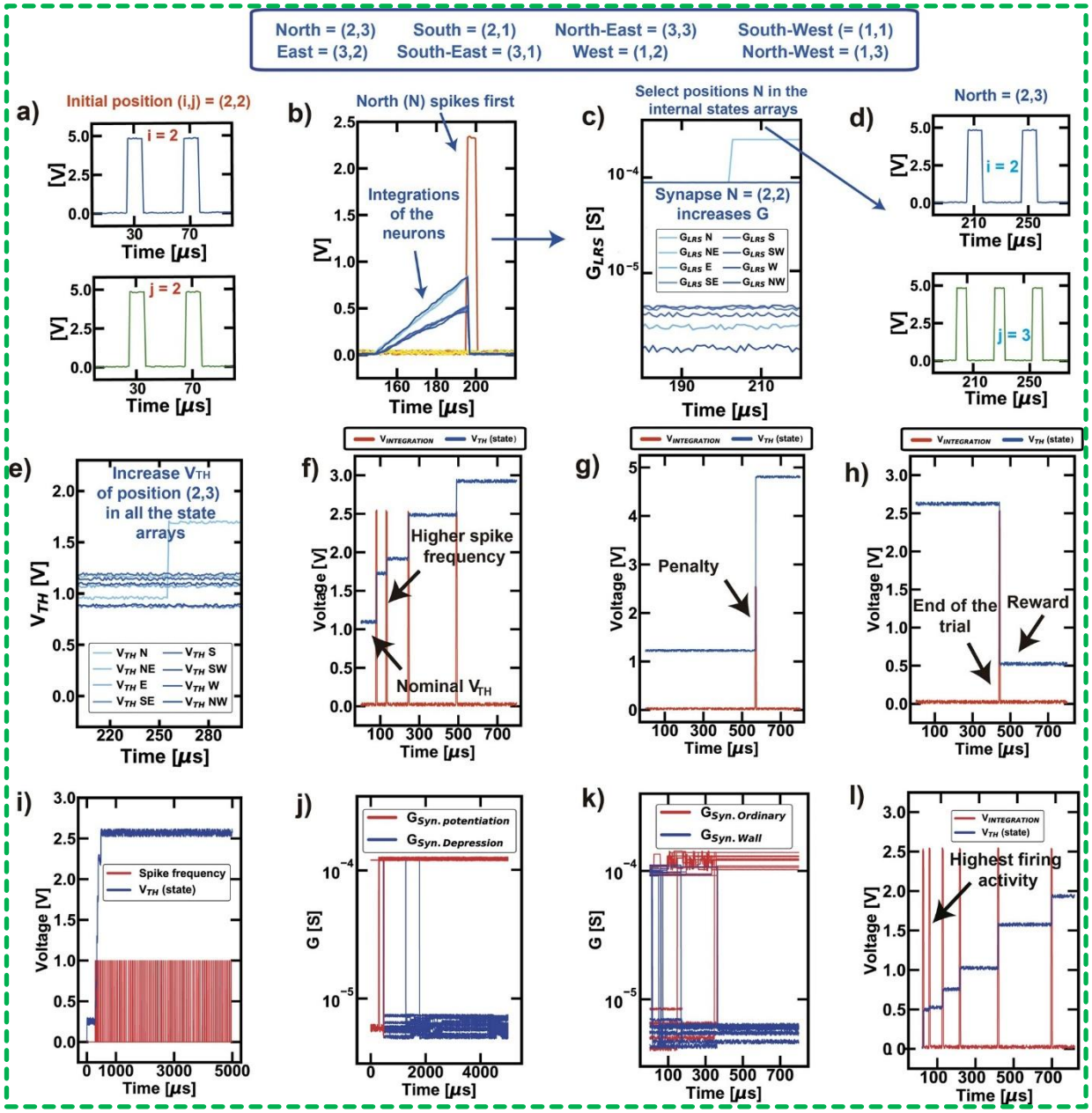

Figure 8(a-l). Activity-dependent internal-state adaptation and homeostatic regulation in RRAM-based neuromorphic hardware, **(a-e)** illustrate the successive hardware operations during autonomous navigation, including synaptic integration, firing, movement and internal-state update, **(f-h)** show adaptive threshold modulation during ordinary activity, penalty and reward conditions, **(i)** demonstrates the physical limit of threshold adaptation imposed by the multilevel RRAM state, **(j-l)** describe synaptic potentiation/depression and the influence of previous reward history on subsequent adaptation [96].

5. Comparative Engineering Metrics: How Should Self-Adaptive Devices be Benchmarked?

Conventional synaptic-device comparisons emphasize energy, speed, endurance, retention, dynamic range, number of conductance states, linearity, symmetry and device-to-device variation [10-18, 23-27, 37-45, 47-56, 98]. These metrics remain essential but are incomplete for W+A hardware. A device can have excellent linear weight updates yet no adaptive state, or poor linearity that is mistakenly interpreted as history-dependent learning. Higher-order adaptivity therefore requires separate metrics that test how conditioning changes the update law.

Figure 9 summarizes the conventional performance space used to evaluate artificial synaptic devices and provides an important baseline for the additional metrics proposed in this review. At system level, non-volatility, high integration density, low power consumption and high operating speed remain central requirements for scalable neuromorphic hardware.

Table 2. Higher-order adaptive functions and representative physical implementations

Function	Minimum evidence	Candidate device physics	Refs
Metaplasticity	conditioning alters later ΔW at matched W	threshold/trap/filament history	[86,87,99]
Consolidation	repetition converts volatile/weak trace to stable state	trap lifetime; network reorganization; volatile to nonvolatile transition	[22,25,88,89]
Adaptive forgetting	retention time depends on history/relevance	diffusion, ion relaxation, shallow/deep traps	[22,25,47-51,88]
Homeostasis	negative feedback limits saturation / restores dynamic range	astrocyte layer, coupled transistor, resource regulation	[84,85,90-92]
Heterosynaptic modulation	one pathway changes plasticity of another	modulatory gate or internal trap population	[67,70,93]
Reconfigurability	same element switches computational role	steep switching + nonvolatile state	[95]
Context-dependent plasticity	sensory context changes later learning response	photocarriers, ions, polarization, molecular dipoles	[72-77]
Learning-to-learn	learning parameters adapt across tasks	hardware plasticity parameters / adaptive state	[94]

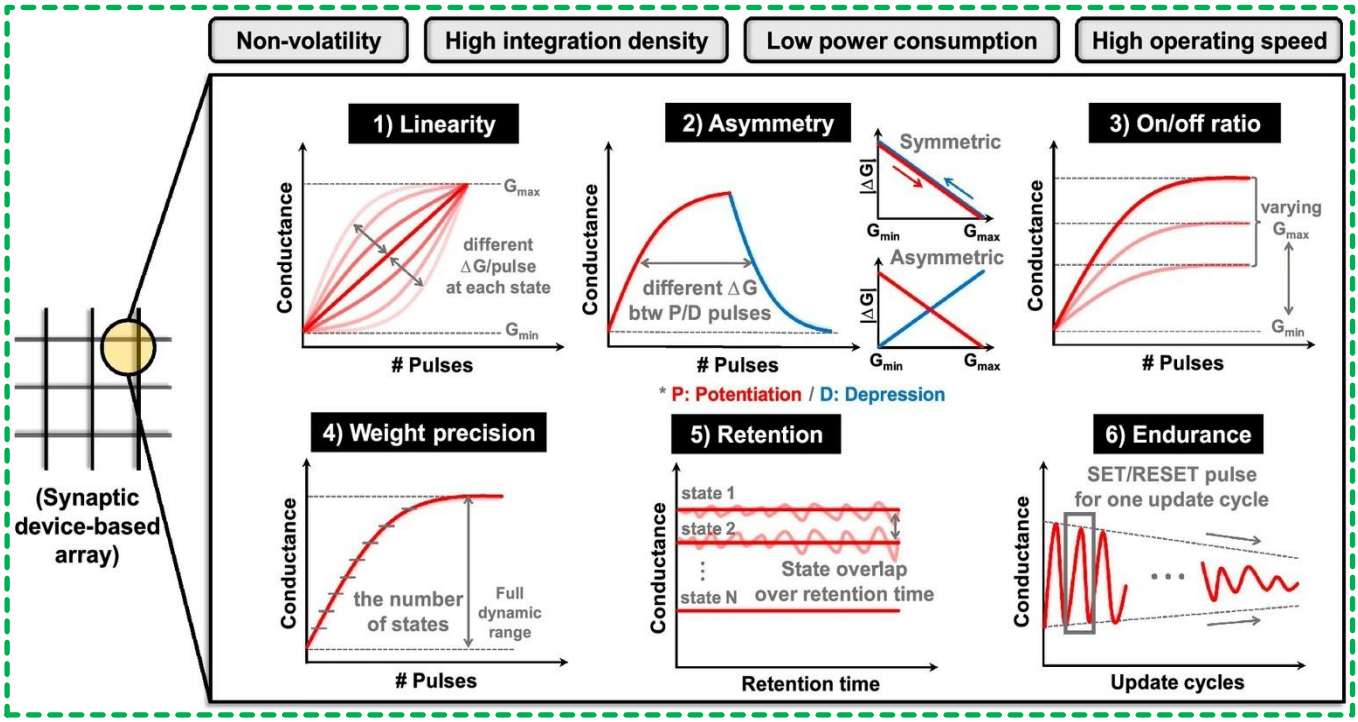

Figure 9. Conventional performance requirements and device metrics for large-scale neuromorphic synaptic hardware. The system-level requirements include non-volatility, high integration density, low power consumption and high operating speed, while device-level evaluation considers programming linearity, potentiation-depression asymmetry, on/off ratio, weight precision, retention and endurance. These established metrics provide the baseline upon which the additional adaptive-state benchmarks proposed in this review are constructed [15].

Table 3. Proposed benchmark set for W+A neuromorphic devices

Metric	Suggested definition	Why it matters
Weight state W	read conductance/current/optical transmission under non-disturbing read	state distribution and read noise
Adaptive gain M	ΔWprobe(after conditioning)/ΔWprobe(control), at matched W	conditioning-dependent change in learning susceptibility
Timescale separation	τA/τW or fitted fast/slow relaxation constants	whether W and A can be functionally separated
Adaptive dynamic range	max(M)/min(M) within reliable operation	strength of learning-rule modulation
Recovery / forgetting	time for M to return toward baseline	reversibility and self-normalization
Cross-talk	unintended change in W while programming A, and vice versa	orthogonality of state control
Adaptive energy	energy to change A by a defined amount	cost of higher-order learning
Cycle reproducibility	distribution of M across conditioning cycles/devices	whether metaplastic behavior is programmable rather than aging
Array locality	number of devices/peripherals needed per adaptive synapse	scalability cost
Task-level benefit	continual-learning retention, calibration reduction, stability or accuracy gain	algorithmic value of A

At device level, linearity determines whether equal programming pulses produce predictable incremental changes in conductance, while potentiation-depression asymmetry determines whether positive and negative weight updates can be implemented without systematic training bias. The on/off ratio defines the available dynamic range, and weight precision determines how many distinguishable intermediate states can be reliably represented within this range. Retention determines whether stored states remain stable over the required operating period, whereas endurance limits the number of repeated learning cycles that can be tolerated. These parameters remain essential for self-adaptive devices, but they do not quantify whether the learning rule itself changes with previous history. Consequently, the conventional metrics shown in Figure 9 should be supplemented by adaptive gain, W-A cross-talk, adaptive-state dynamic range, timescale separation, recovery kinetics, conditioning endurance and task-level benefit, as proposed in Table 3. The combination of established device metrics and higher-order adaptive metrics provides a more rigorous basis for comparing self-adaptive neuromorphic platforms [15].

5.1 Avoiding Misleading Comparisons

Reported energy numbers are often not directly comparable because some include only the active device pulse while others include peripheral circuitry; retention is measured at different temperatures and read biases; and conductance-state counts may be extracted under different noise criteria [12, 15, 16, 45, 52-56]. The same caution is even more important for adaptive-state claims. A metaplasticity curve should not be compared across devices without stating the conditioning protocol, initial W, probe amplitude, delay after conditioning, and whether the adaptive effect persists after the conditioning signal is removed. It is recommended reporting both device-only and estimated system-level costs whenever possible.

6. Device-Circuit-Algorithm Co-Design for Adaptive Learning

6.1 Why the Algorithm must know which Physics is useful

Analog memory research has repeatedly shown that hardware-aware algorithms can convert device imperfections into usable computation, whereas

blindly mapping software weights to devices often fails because of asymmetry, variability and drift [18, 24, 26, 27, 38, 41]. The same principle applies to W+A devices. The algorithm should not demand a perfectly independent A if the physics naturally couples A and W; instead it should exploit the coupling in a stable learning rule. For example, a slow ionic or trap state could implement a local learning-rate schedule, a homeostatic target, a novelty signal or an eligibility trace rather than a second conventional memory bit.

6.2 Continual Learning and Catastrophic Forgetting

A central motivation for adaptive hardware is continual learning. Conventional analog synapses overwrite weights when new tasks arrive. A slow state A can protect consolidated weights, decrease the update rate of stable features, or selectively increase plasticity for novel patterns. This resembles metaplastic and consolidation mechanisms in neuroscience [83-85, 88, 89] and hardware learning-to-learn concepts [94]. A useful benchmark is therefore not only MNIST inference accuracy but performance under sequential tasks, domain shift, few-shot adaptation, or nonstationary sensory statistics.

6.3 Local Homeostasis as a Hardware Calibration Mechanism

Device variation forces large arrays to use write-verify, redundancy or algorithmic calibration [18, 23, 26, 27, 38, 54]. A self-regulating A state could reduce this overhead by locally adjusting programming sensitivity when W approaches saturation or when a device becomes unusually responsive. Astrocyte-inspired and tripartite architectures are early demonstrations of this direction [90-92]. The practical success criterion is not biological resemblance but whether the extra state reduces peripheral complexity, training energy or accuracy loss at array scale.

7. A Five-Level Hierarchy for Evaluating Neuromorphic Device Intelligence

Level 1 - Memory: Stores discrete or analog state but has no learning dynamics beyond programming. Flash, RRAM, PCM, FeRAM used as conventional memory.

Level 2 - Plastic Synapse: Input history changes W according to a fixed device response. LTP/LTD, STDP, PPF, analog weight update.

Level 3 - Adaptive Synapse: Recent history changes retention, volatility or update magnitude. Volatile-to-nonvolatile transition, adaptive forgetting, consolidation.

Level 4 - Self-Adaptive Synapse: A separable state a changes the future learning rule and can recover or be regulated. Metaplasticity, homeostasis, modulatory-gate control.

Level 5 - Self-Evolving Neuromorphic system: Networks exploit adaptive states to alter learning strategy across contexts/tasks. Learning-to-learn, continual adaptation, sensor-context-dependent learning.

The purpose of the hierarchy is not to rank materials but to prevent functional inflation. A Level-4 claim should require evidence that the learning rule changes, not merely that the conductance is multilevel. Conversely, a simple material system can be Level 4 if it has a robust adaptive state, while a complex heterostructure may remain Level 2 if all internal physics collapses into a fixed conductance-update curve. Existing metaplastic, homeostatic and reconfigurable demonstrations suggest that Levels 3-4 are experimentally reachable [67-77, 86-95, 97, 99], whereas Level 5 will require coordinated device, circuit and algorithm design [8, 94].

8. Major Challenges Before Self-Adaptive Devices Become Useful Hardware

The most fundamental challenge is state identifiability. In many neuromorphic devices, several microscopic variables contribute to the same terminal conductance, and a measured current does not uniquely reveal the internal configuration. Filament radius, gap distance, ion concentration, trap occupancy, polarization distribution, crystallized fraction, and local temperature history can all create memory effects that appear similar in an electrical sweep [22, 25, 28, 37-45, 47-56, 59, 67-70]. This creates a serious problem for claims of self-adaptation because ordinary state-dependent switching may be mistaken for a separate adaptive state. The appropriate test is not simply to show that a device responds differently after different pulse trains. Instead, two histories should be prepared that finish at approximately the same W, followed by an identical probe sequence. A statistically significant difference in the subsequent update trajectory provides stronger evidence that another state variable is present. Operando microscopy, spectroscopic probes, transient current analysis, temperature dependence, pulse-relaxation experiments, and compact modeling can then be used to identify the physical carrier of A. Causal perturbation is especially important: if a proposed ion distribution or trap population is responsible for adaptation, selectively changing that variable while minimally changing W should alter the next learning response. Without this level of control, higher-order terminology can obscure rather than clarify the device physics.

A second challenge is engineering the separation of time scales. Self-adaptation requires at least two forms of memory with different kinetics, but

the useful ratio between those time constants depends strongly on the target application. Diffusive memristors, volatile ionic devices, and electrochemical transistors can naturally generate fast and slow components through different diffusion lengths, binding energies, reservoirs, or redox pathways [22, 25, 47-56]. PCM and ferroelectric devices provide more persistent states, but their structural relaxation, drift, domain-wall dynamics, trapping, and thermal or electric-field history can introduce slower secondary variables [37-45, 59-62, 97]. If the adaptive state changes almost as rapidly as W, it becomes difficult to identify or exploit independently. If it is too slow, the device cannot modify its learning rule within the time horizon of the task. The optimal design is therefore application-specific. Sensor adaptation may tolerate seconds or hours, whereas on-chip training may require adaptive changes over microseconds to milliseconds. This creates a materials design problem that is more demanding than conventional retention optimization: the goal is not simply the longest possible memory, but a controlled hierarchy of volatility, consolidation, and recovery times that matches the statistics of the workload.

Variability becomes more complex when a second state is introduced. Filamentary RRAM already exhibits cycle-to-cycle and device-to-device variation because switching depends on stochastic nucleation, defect distribution, and local Joule heating [17, 18, 23-28, 32-36]. PCM introduces stochastic crystallization and resistance drift, while ECRAM depends on ionic conductivity, reservoir balance, electrolyte quality, and interfacial electrochemistry [37-45, 47-56]. Ferroelectric devices are affected by domain nucleation statistics, imprint, depolarization, trapping, wake-up, and fatigue [59-66]. In a W+A device, variation can occur not only in the stored weight but also in adaptive gain, recovery time, threshold, and cross-coupling between the two states. This is potentially harmful because a learning algorithm may see each cell as having a different learning rule. At the same time, controlled heterogeneity can be computationally useful for reservoir computing, temporal processing, or population coding. The engineering objective should therefore be to distinguish useful diversity from uncontrolled variation. Reports should provide distributions for both the immediate weight update and the conditioned update response, including repeated conditioning-recovery cycles. A particularly attractive direction is local self-calibration, where devices with excessive programming sensitivity automatically reduce their update gain while less responsive devices increase it, converting part of the variability problem into a homeostatic function [84, 90-92].

Reliability and endurance must also be reconsidered because adaptive operation can require additional state transitions beyond ordinary weight programming. Ionic and electrochemical devices may suffer from irreversible side reactions, reservoir depletion, electrolyte decomposition, delamination, or slow compositional drift when repeatedly driven through large chemical windows [47-56]. Filamentary devices can accumulate structural damage or electrode reactions, PCM can experience thermal stress and composition-related aging, and ferroelectric devices can show cycling-related fatigue or charge-trapping evolution [37-46, 59-62, 97]. A device may therefore demonstrate impressive metaplasticity over a small number of laboratory pulse trains while losing the adaptive response after prolonged operation. Endurance testing should track not only resistance-window failure but also whether the adaptive-state amplitude, time constant, and reversibility remain stable. The same principle applies to retention: a stable W does not guarantee a stable learning rule if A drifts unpredictably. Reliability specifications for self-adaptive hardware should consequently include adaptive-state retention, conditioning endurance, recovery repeatability, and the effect of temperature and bias history on both W and A.

Array integration creates another major competitive trade-off between density and control. Two-terminal RRAM and PCM can achieve compact crossbar layouts but provide limited access to hidden internal variables, and large arrays additionally suffer from sneak paths, line resistance, write disturbance, selector constraints, and conductance-dependent sensing [11, 12, 16-20, 26, 27, 32-36, 38, 64-66,100]. Three-terminal ECRAM, OECT, FeFET, and 2D synaptic transistors offer cleaner separation between read and write paths and may allow a dedicated terminal to control A, but every additional terminal increases routing area and peripheral complexity [47-56, 59-62, 67-70, 97, 98]. Multimodal devices may require optical access, specialized encapsulation, or sensor-specific interfaces [71-77]. Consequently, the smallest device is not automatically the most area-efficient adaptive system. The relevant comparison should include access transistors, selectors, row and column drivers, ADCs and DACs, sensing precision, refresh, write-verify, calibration memory, and additional control lines. An adaptive mechanism is most compelling when it removes a larger amount of digital support than it adds. For example, local homeostasis that prevents saturation could be valuable if it reduces repeated global recalibration, whereas an A state that requires high-resolution readout and a separate closed-loop controller may simply relocate the computational burden.

Energy and speed claims require similarly careful normalization. Neuromorphic papers often report the energy of the active device pulse, while system performance is governed by the combined cost of driving interconnects, generating analog voltages, reading small currents, converting signals, and performing write-verify operations [12, 15, 16, 45, 52-

56]. Self-adaptive hardware introduces at least one additional operation: conditioning, setting, reading, or recovering A. The appropriate figure of merit should therefore distinguish energy per weight update from energy per adaptive-state transition and should report whether the adaptive function reduces the number of subsequent writes, calibration cycles, or external computations. Latency should also be separated into pulse duration, physical relaxation time, verification time, and array communication. A slow physical process can still be useful if it occurs asynchronously in the background of a sensor or if it replaces frequent digital updates, whereas the same process may be unacceptable in a high-throughput accelerator. Competitive comparisons should therefore be performed at task level and should include the peripheral energy and time needed to exploit the adaptive state.

Finally, benchmark fragmentation currently prevents rigorous comparison across material platforms. Conventional studies often use different pulse amplitudes, widths, initial conductance windows, retention conditions, state-count definitions, and neural-network simulations [15-18, 23-27, 45, 52-56]. Higher-order adaptive claims add conditioning history as another uncontrolled variable. A useful minimum benchmark should include a conditioning-probe experiment at matched W, a dose-response curve showing how A depends on conditioning strength, recovery kinetics after conditioning is removed, repeated-cycle statistics, and a measure of cross-talk showing how much W changes while A is programmed. Consolidation should be evaluated under spaced and massed training, homeostasis should be tested by deliberately driving weights toward saturation and measuring recovery, and continual-learning demonstrations should use sequential tasks rather than a single static classification dataset [86-95, 99]. Device-only metrics should be accompanied by array-aware simulations or hardware measurements that include realistic variation and peripheral constraints. Such standardized experiments would make it possible to distinguish devices that merely exhibit complex hysteresis from those that provide a robust, controllable, and computationally useful learning-rule state.

9. Future Scope and Research Opportunities

The most promising future direction is the deliberate design of physically orthogonal dual-state devices rather than the accidental use of uncontrolled internal history. W and A should ideally be associated with different but coupled degrees of freedom so that each can be addressed with limited cross-talk. Electrochemical devices could combine fast channel doping with a slower reservoir or interfacial chemical state; ferroelectric devices could combine polarization with trapping or ionic redistribution; and multi-terminal transistors could assign the primary weight to channel conductance while a separate gate stores a modulatory state [48-56, 59-62, 67-70, 97, 98]. The degree of orthogonality should be quantified experimentally through a cross-talk matrix that measures how programming W affects A and how programming A perturbs W. This would move the field beyond qualitative claims of multiple mechanisms and toward reproducible multi-state engineering. Hybrid stacks may be particularly useful when the two mechanisms have naturally separated activation energies or response times, but material compatibility, fabrication temperature, and endurance must be considered from the beginning rather than after a single-device demonstration.

A second opportunity is to replace the conventional goal of maximum retention with adaptive retention. Many edge-learning tasks do not require every event to be stored permanently. Weak or isolated inputs can remain volatile, while repeated, correlated, or rewarded inputs can progressively recruit a more stable state [22, 25, 88, 89]. Diffusive memristors and electrochemical systems are well suited to this concept because relaxation can be tuned through ion mobility, binding sites, geometry, or reservoir coupling, whereas PCM and ferroelectric devices can provide a stronger nonvolatile anchor [37-45, 47-56, 59-62]. Such devices could implement consolidation without transferring data between separate short-term and long-term memories. An important research question is whether the energy saved by allowing unimportant states to decay outweighs the overhead of maintaining the consolidation mechanism. Experiments should therefore compare fixed-retention and adaptive-retention devices under identical continual-learning workloads and quantify write count, accuracy retention, energy, and memory capacity.

Local homeostatic regulation is another high-value direction because it links higher-order plasticity directly to a practical array problem. Analog synaptic arrays lose effective resolution when weights crowd near the upper or lower conductance limits, and device variation causes different cells to respond unequally to the same programming pulse [18, 23, 26, 27, 38, 54]. A slow adaptive state could act as negative feedback by reducing update sensitivity near saturation, shifting the local operating point, or increasing plasticity in insensitive cells. Astrocyte-inspired and tripartite approaches already illustrate the concept of regulatory feedback [90-92]. Future work should integrate this behavior into realistic crossbars and determine whether physical homeostasis can reduce write-verify frequency, calibration memory, ADC precision, or training instability. The key comparison is not whether the device reproduces an astrocyte-like waveform, but whether its local regulation produces a measurable

system-level reduction in overhead or variation-induced accuracy loss.

Context-gated sensory learning offers a different route in which A is written by the environment rather than by the same electrical pulses used to store W. Optoelectronic and multimodal devices can respond to wavelength, light intensity, chemical species, mechanical input, polarization, or other sensory variables [71-77]. If these signals only change the instantaneous read current, the device functions as a sensor with memory. A more powerful architecture would allow the contextual signal to alter subsequent electrical plasticity even after the context has been removed. For example, optical exposure could temporarily increase or suppress electrical learning rate, or a chemical input could set the retention time of a later electrical event. Such context-dependent plasticity could reduce the need for a digital controller that separately classifies context and then modifies the learning algorithm. Future studies should use matched-W tests to distinguish genuine context-gated learning from photoconductive or sensing hysteresis and should evaluate the function under time-varying real-world input rather than only repeated laboratory pulses.

Device-level metaplasticity can also be connected more directly with continual learning and hardware meta-learning. In this approach, W serves as a fast task-specific variable while A accumulates slower information about stability, novelty, confidence, or past task statistics [83-90, 93, 94, 99]. An algorithm could use A to reduce updates to consolidated features, increase plasticity for novel inputs, allocate learning resources, or implement local learning-rate schedules. This is conceptually different from storing two ordinary weights because the slower variable modifies the rule used to update the faster one. Hardware demonstrations should therefore move beyond static image classification and evaluate sequential tasks, domain shifts, few-shot adaptation, and recovery after distribution changes. The strongest evidence would be a comparison in which the same array is operated with and without the adaptive state while all other conditions are held constant. Such experiments would reveal whether device physics genuinely mitigates catastrophic forgetting or merely adds another tunable parameter that could have been implemented digitally at lower cost.

Materials and integration research should simultaneously target scale, manufacturability, and controllability. ECRAM and OECT devices need solid electrolytes, stable interfaces, and scalable geometries that preserve ion-control advantages at small dimensions [45, 52-56]. Ferroelectric systems require control of wake-up, fatigue, imprint, trapping, and domain statistics while maintaining analog tunability at technologically relevant dimensions [59-66]. Two-dimensional and multimodal devices must address contact resistance, transfer contamination, encapsulation, uniformity, and wafer-scale process compatibility [67-77]. RRAM and PCM remain attractive because of their maturity and density, but adaptive functions should be engineered without sacrificing selector compatibility, endurance, or crossbar yield [19, 20, 29-46, 64-66,100]. Vertical integration and heterogeneous 3D architectures may eventually allow a fast weight layer, a slower adaptive layer, and local sensing circuitry to be stacked rather than routed laterally [103]. The most competitive architecture will therefore be determined by system integration, not by isolated device functionality alone.

Progress will also depend on better models and shared data. Most compact models describe conductance as a function of applied voltage and one internal state, which is insufficient for a device whose future update response depends on a second history variable [28, 100]. Models should explicitly include W, A, their coupling, their characteristic time scales, stochastic terms, temperature dependence, and saturation or recovery mechanisms. Experimental datasets should contain raw pulse trains, intermediate read states, conditioning histories, delays, temperature, device identifiers, and repeated-cycle statistics so that algorithms can be tested using realistic adaptive dynamics rather than idealized update equations. A common benchmark library could provide standard conditioning-probe protocols, consolidation tests, homeostatic recovery tests, and sequential-learning tasks. Open models and datasets would also make it easier to compare whether a complex adaptive device outperforms a simpler memory cell combined with digital control.

A final research opportunity is to treat adaptive state as a reliability resource. Because A records aspects of recent electrical, thermal, chemical, or sensory history, it could potentially indicate abnormal stress, aging, or drift before W fails. The same mechanism used for learning-rate regulation could be designed to compensate gradual sensitivity changes, reduce programming stress, or trigger local recalibration. This requires clear separation between computational adaptation and irreversible degradation, but it offers a practical route toward self-monitoring analog hardware. Future studies should therefore report how adaptive behavior evolves with cycling and aging and should test whether the device can use its own history state to preserve useful operating margins. If successful, self-adaptive neuromorphic devices could combine learning, stabilization, and health monitoring in the same physical substrate rather than treating reliability as an external maintenance function.

10. Conclusion

This review highlights the transition of neuromorphic hardware from conventional memory

and first-order synaptic plasticity toward self-adaptive devices capable of modifying not only their conductance state but also their future learning response. Across memristive, phase-change, electrochemical, ferroelectric, two-dimensional, and transistor-based platforms, a common limitation is that most devices still encode learning through a single effective state variable, while biological adaptation relies on multiple interacting processes operating over different timescales. The proposed weight-adaptation framework addresses this gap by distinguishing the stored synaptic weight from an additional adaptive state that regulates update sensitivity, retention, forgetting, consolidation, and subsequent plasticity. Such separation provides a physically meaningful route toward hardware metaplasticity, homeostatic regulation, experience-dependent learning rates, and context-sensitive memory. From a device perspective, the main challenge is to realize two or more controllable internal states with sufficient independence, linearity, symmetry, endurance, low programming energy, and low device-to-device variation. From a system perspective, the benefit of added adaptivity must outweigh the complexity introduced by extra terminals, control pulses, sensing circuitry, and calibration overhead. Future progress therefore requires closer device-circuit-algorithm co-design, standardized benchmarks for adaptive-state observability, and quantitative comparison of timescale separation, retention tunability, update nonlinearity, and energy efficiency. If these issues are addressed, self-adaptive neuromorphic devices could move beyond static weight storage toward hardware that continuously regulates how it learns, remembers, forgets, and responds to changing environments, enabling more autonomous and biologically plausible computing systems.

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Conflict of interest

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Yes.

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