

Design and Analysis of 31-Level Asymmetric Cascaded H-Bridge Multilevel Inverter with Reduced Number of Switches

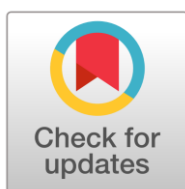
A. Manoranjan ^{a,*}, C. Christober Asir Rajan ^a

^a Department of Electrical and Electronics Engineering, Pondicherry Engineering College, Puducherry, Tamil Nadu, India.

* Corresponding Author: vjcmano@gmail.com DOI: <https://doi.org/10.34256/bsr2023>

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Abstract: A new multilevel inverter with less no of power switches is proposed. This is based on cascaded H-bridge topology. The design and analysis of 31-level reduced switch inverter with different modes of operation are presented in this paper. The proposed inverter is asymmetric in nature and it uses unequal DC voltage sources. PD-PWM modulation technique has been used here to get proper switching. The proposed idea has been validated through simulation and the received results provides better efficiency, less low order harmonics and less switching losses.

Keywords: Multilevel Inverter (MLI), Phase Disposition Pulse Width Modulation (PD-PWM), Cascaded H-bridge, Total Harmonic Distortion (THD).

1. Introduction

Multilevel inverter is a new domain of power converters used extensively in high and medium power applications such as integration of renewable energy resources, FACTS devices and so on [1-3]. The obtained output voltage waveform is nearly sinusoidal. In power electronic applications multilevel inverters are becoming popular as they have the good ability to meet the more demand of power rating and power quality associated with reduced harmonic distortion and lower electromagnetic interference. Multilevel inverter has the ability to operate with both fundamental and high switching frequency [1,5-9]. Basically, there are three different topologies employed for Multilevel inverter: Neutral point clamp MLI (NPC), Flying capacitor MLI (FC) and Cascaded H-bridge MLI (CHB) [1, 10]. In this the Cascaded H-bridge topology has gained a lot of interest because of its simplicity and modularity with the limitation of separate DC sources for each

module when compared with other topologies such as NPC and FC [1].

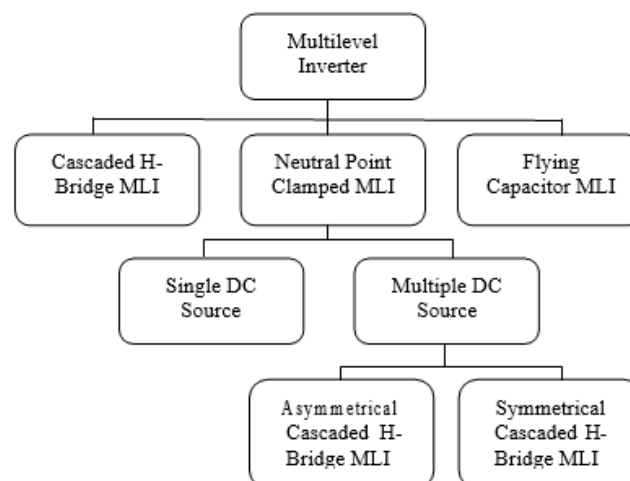


Fig 1. Flow Chart of MLI Topologies.

On the basis of magnitude of DC voltages, CHB topology fall into two categories: Symmetric CHB and Assymetric CHB. The asymmetric topology utilizes a smaller number of switches, DC sources and diodes for same

voltage levels as compared to symmetric topology [1]. The proposed MLI topology has more advantages than the existing topologies as the number of switching devices and total harmonic distortion are reduced.

In asymmetric multilevel inverter, DC source magnitudes are unequal and it is designed as to maintain a ratio of 1:2:4:8 [11-16]. A 2Khz multiple carrier signal is used to develop phase disposition pulse width modulation (PD-PWM). In this paper, level shifted PWM topologies with reduced no of switches which uses separate DC sources has been designed. The no of switches and no of levels are represented as follows

$$N_{Level} = 2(n+1) - 1$$

$N_{MOSFET} = n+4$ where n- no of DC sources.

The DC source magnitudes are designed with binary form of voltage such as 3V, 6V, 12V and 24V.

2. Proposed System

This section presents a detailed description of the proposed system which has additional features with added flexibility to that of the existing systems.

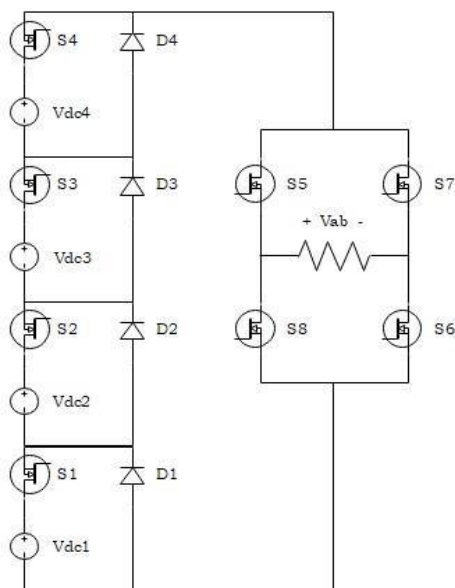


Fig 2. Block Diagram of Proposed System.

It is implemented with a set of switch, diode and DC source at the input side of the circuit which produces higher output voltage level.

3. Switching Modes of Operation

Based on the gating signals, the four MOSFET switches in different times to create 31 different voltage levels which are shown in this section.

Table 1. Switching Order of MOSFET's Based on Gate Signals

Vo	S1	S2	S3	S4	S5	S6	S7	S8
Vdc	1	1	1	1	1	1	0	0
14Vdc/15	0	1	1	1	1	1	0	0
13Vdc/15	1	0	1	1	1	1	0	0
12Vdc/15	0	0	1	1	1	1	0	0
11Vdc/15	1	1	0	1	1	1	0	0
10Vdc/15	0	1	0	1	1	1	0	0
9Vdc/15	1	0	0	1	1	1	0	0
8Vdc/15	0	0	0	1	1	1	0	0
7Vdc/15	1	1	1	0	1	1	0	0
6Vdc/15	0	1	1	0	1	1	0	0
5Vdc/15	1	0	1	0	1	1	0	0
4Vdc/15	0	0	1	0	1	1	0	0
3Vdc/15	1	1	0	0	1	1	0	0
2Vdc/15	0	1	0	0	1	1	0	0
Vdc/15	1	0	0	0	1	1	0	0
0	0	0	0	0	1	0	1	0
0	0	0	0	0	0	1	0	1
-Vdc/15	1	0	0	0	0	0	1	1
-2Vdc/15	0	1	0	0	0	0	1	1
-3Vdc/15	1	1	0	0	0	0	1	1
-4Vdc/15	0	0	1	0	0	0	1	1
-5Vdc/15	1	0	1	0	0	0	1	1
-6Vdc/15	0	1	1	0	0	0	1	1
-7Vdc/15	1	1	1	0	0	0	1	1
-8Vdc/15	0	0	0	1	0	0	1	1
-9Vdc/15	1	0	0	1	0	0	1	1
-10Vdc/15	0	1	0	1	0	0	1	1
-11Vdc/15	1	1	0	1	0	0	1	1
-12Vdc/15	0	0	1	1	0	0	1	1
-13Vdc/15	1	0	1	1	0	0	1	1
-14Vdc/15	0	1	1	1	0	0	1	1
-Vdc	1	1	1	1	0	0	1	1

Mode 1:

Switch S1, S2, S3, S4, S5 and S6 is ON, the voltage is maximum +Vdc across the load.

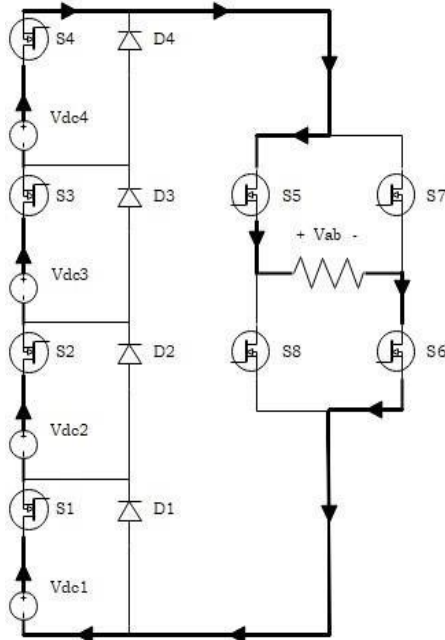


Fig 3. Mode 1

Mode 3:

Switch S1, S3, S4, S5 and S6 is ON, the voltage is +13Vdc/15 across the load.

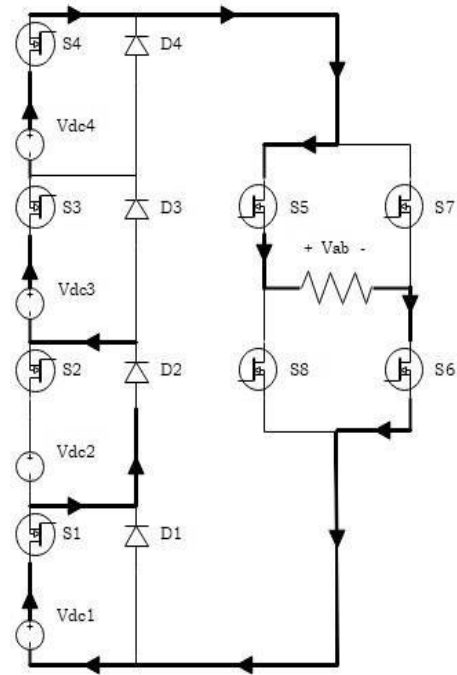


Fig 5. Mode 3

Mode 2:

Switch S2, S3, S4, S5 and S6 is ON, the voltage is +14Vdc/15 across the load

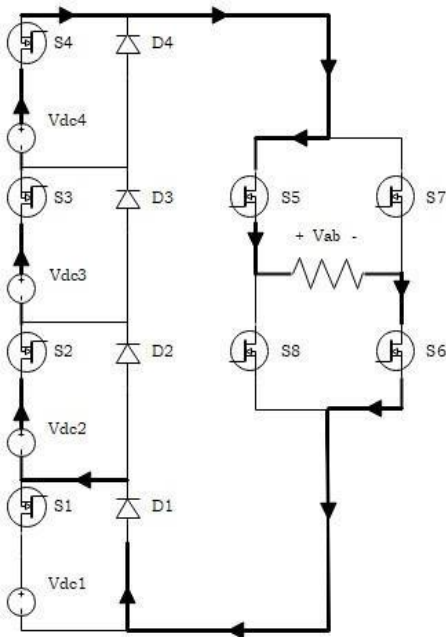


Fig 4. Mode 2

Mode 4:

Switch S3, S4, S5 and S6 is ON, the voltage is +12Vdc/15 across the load.

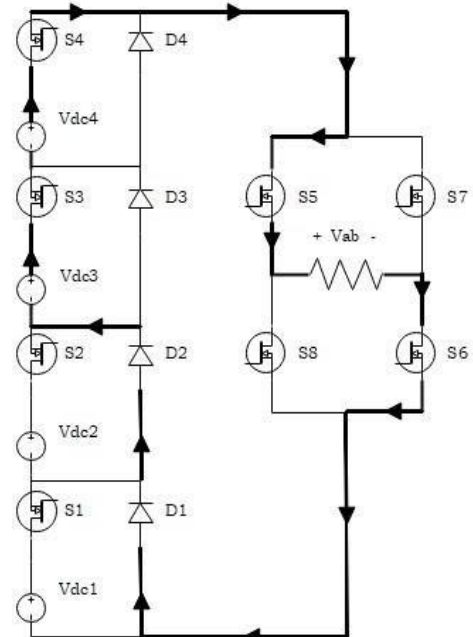


Fig 6. Mode 4

Mode 5:

Switch S1, S2, S4, S5 and S6 is ON, the voltage is +11Vdc/15 across the load.

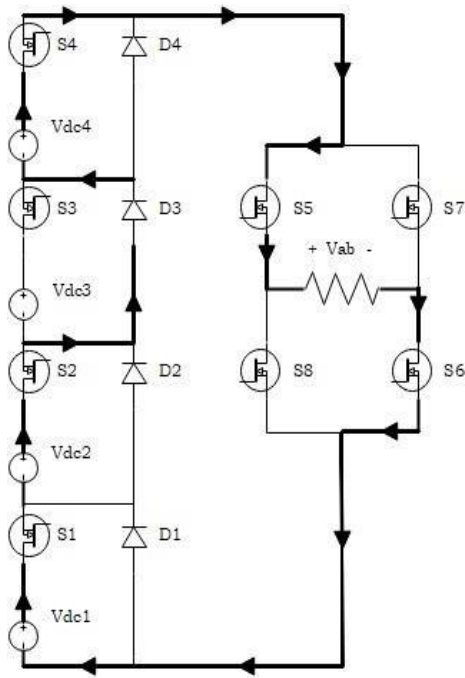


Fig 7. Mode 5

Mode 7:

Switch S1, S4, S5 and S6 is ON, the voltage is +9Vdc/15 across the load.

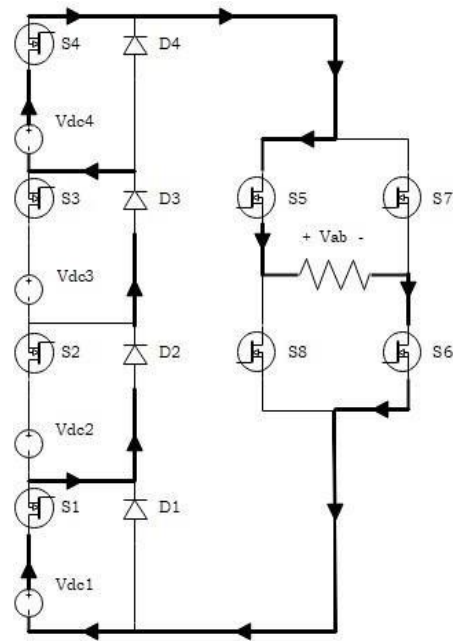


Fig 9. Mode 7

Mode 6:

Switch S2, S4, S5 and S6 is ON, the voltage is +10Vdc/15 across the load.

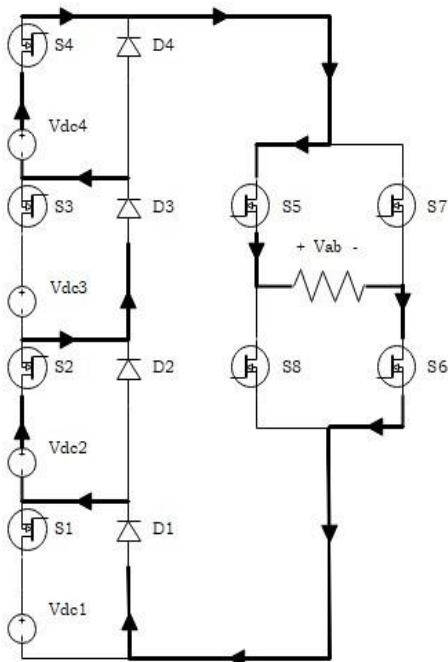


Fig 8. Mode 6

Mode 8:

Switch S4, S5 and S6 is ON, the voltage is +8Vdc/15 across the load.

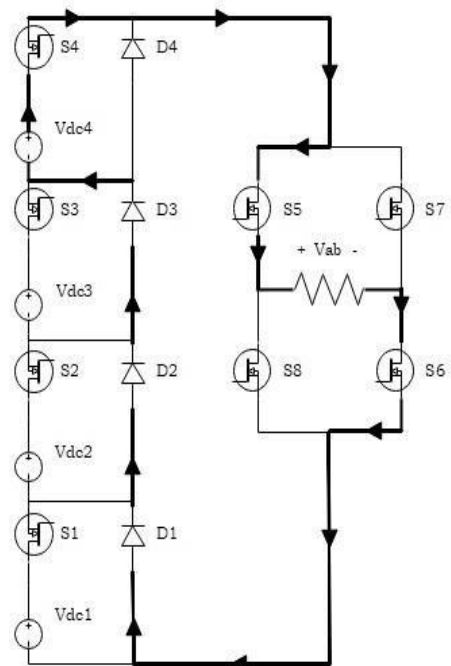


Fig 10. Mode 8

Mode 9:

Switch S1, S2, S3, S5 and S6 is ON, the voltage is $+7V_{dc}/15$ across the load.

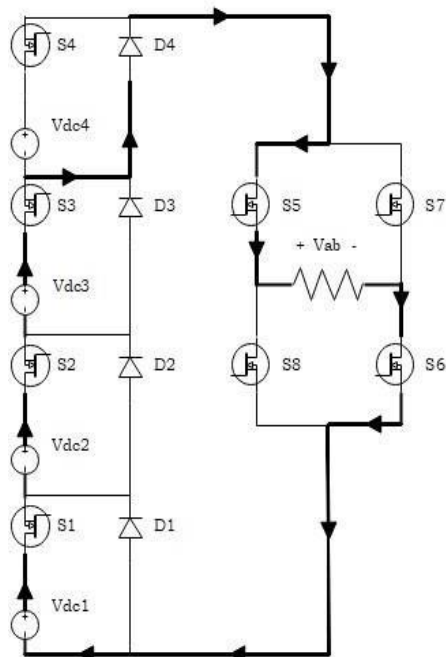


Fig 11. Mode 9

Mode 11:

Switch S1, S3, S5 and S6 is ON, the voltage is $+5V_{dc}/15$ across the load.

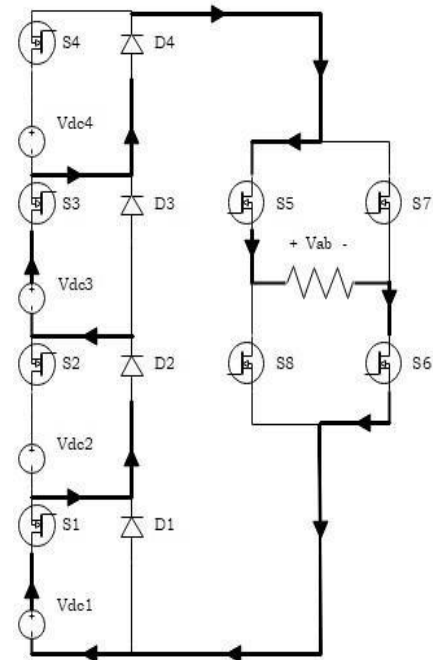


Fig 13. Mode 11

Mode 10:

Switch S2, S3, S5 and S6 is ON, the voltage is $+6v_{dc}/15$ across the load.

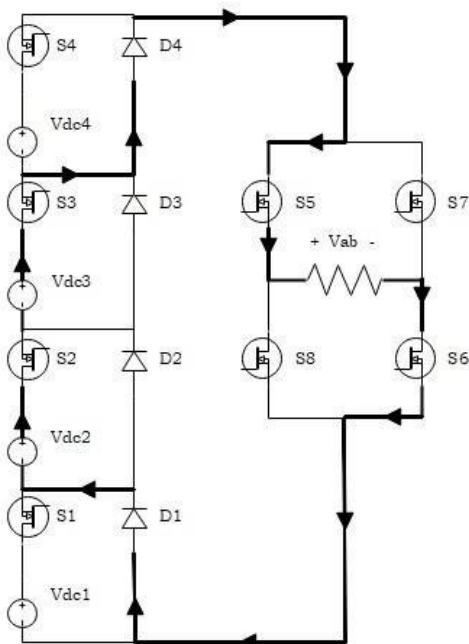


Fig 12. Mode 10

Mode 12:

Switch S3, S5 and S6 is ON, the voltage is $+4V_{dc}/15$ across the load.

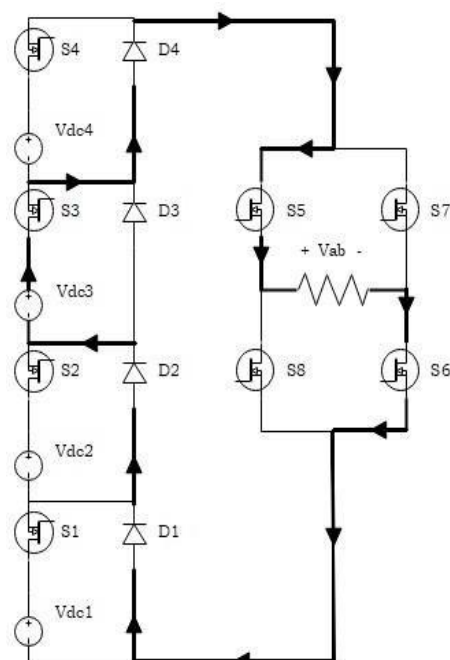


Fig14. Mode 12

Mode 13:

Switch S1, S2, S5 and S6 is ON, the voltage is $+3V_{dc}/15$ across the load.

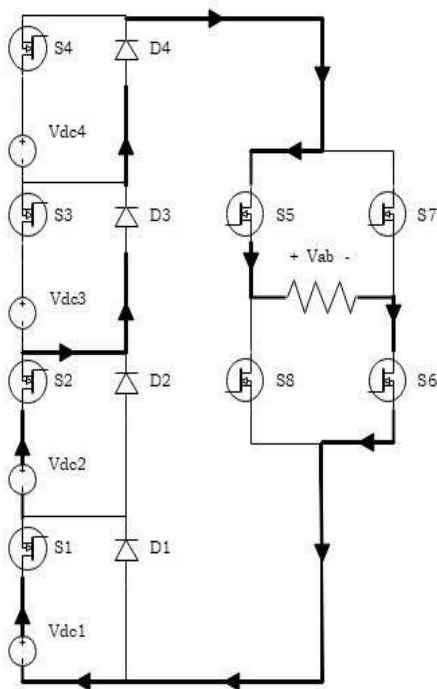


Fig15. Mode 13

Mode 15:

Switch S1, S5 and S6 is ON, the voltage is $+V_{dc}/15$ across the load.

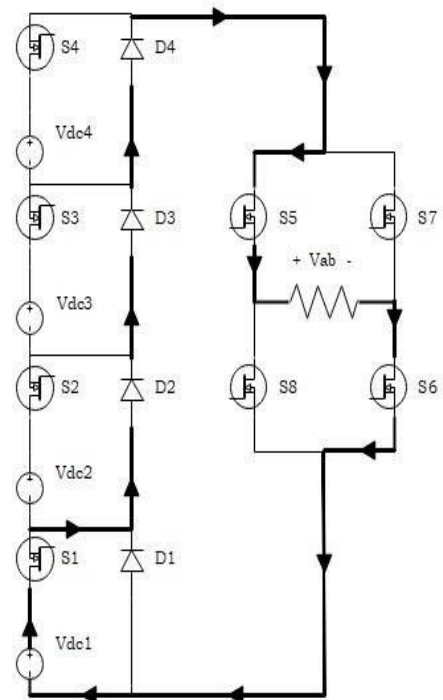


Fig 17. Mode 15

Mode 14:

Switch S2, S5 and S6 is ON, the voltage is $+2V_{dc}/15$ across the load.

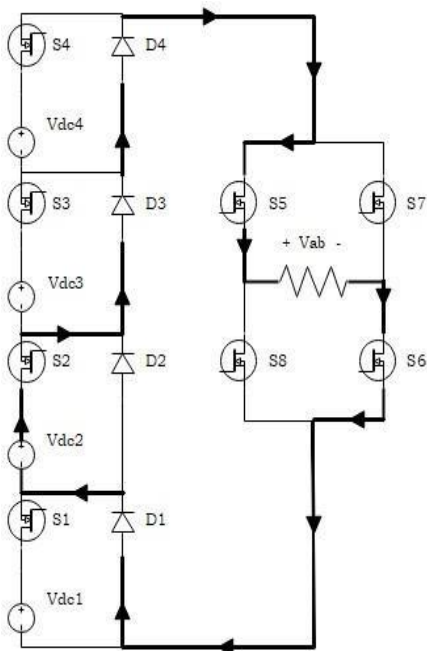


Fig 16. Mode 14

Mode 16a:

The zero-output voltage level is produced by turning ON switch S5 and S7.

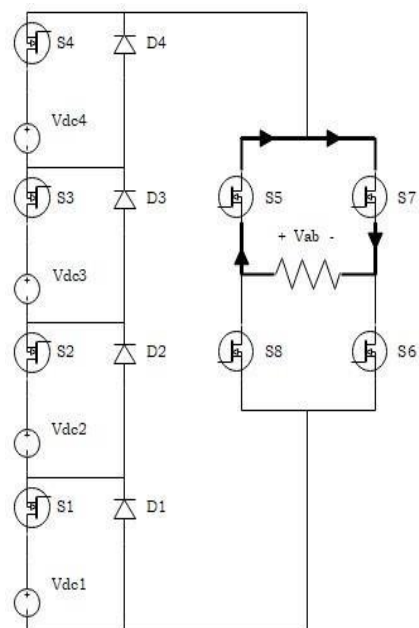


Fig 18. Mode 16a

Mode 16b:

The zero-output voltage level is produced by turning ON switch S6 and S8.

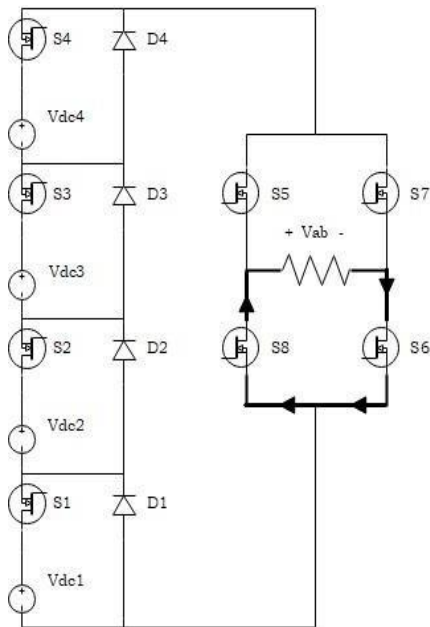


Fig 19. Mode 16b

Mode 18:

Switch S2, S7 and S8 is ON, the voltage is $-2V_{dc}/15$ across the load.

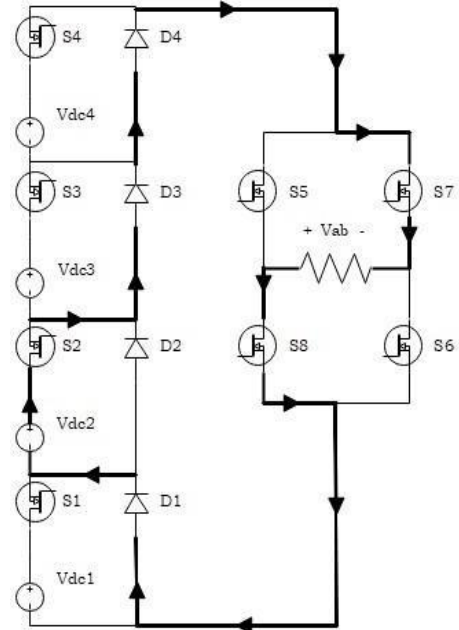


Fig 21. Mode 18

Mode 17:

Switch S1, S7 and S8 is ON, the voltage is $-V_{dc}/15$ across the load.

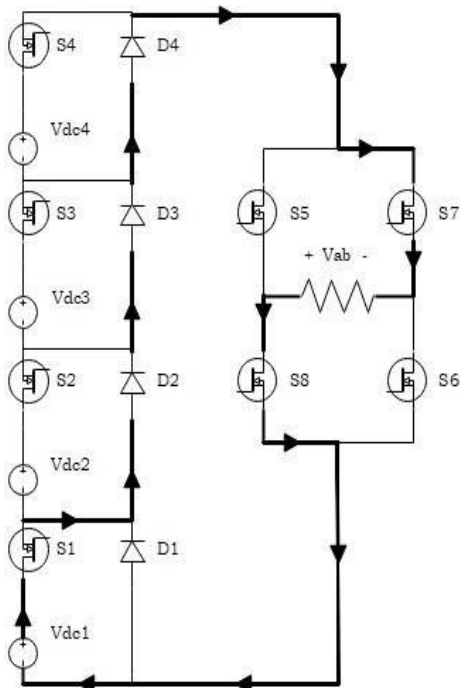


Fig 20. Mode 17

Mode 19:

Switch S1, S2, S7 and S8 is ON, the voltage is $-3V_{dc}/15$ across the load.

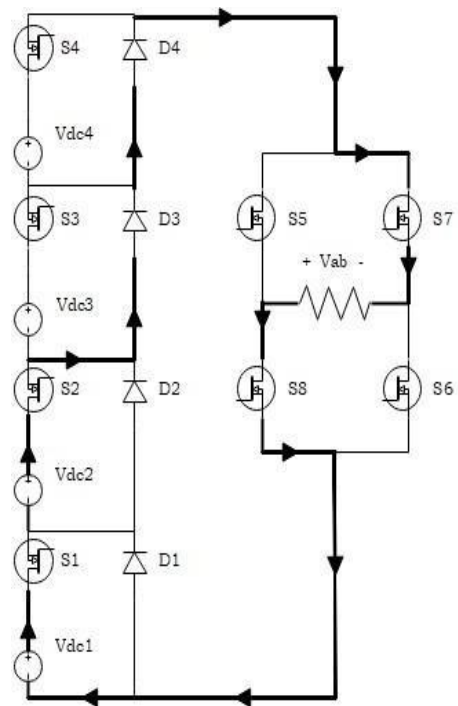


Fig 22. Mode 19

Mode 20:

Switch S3, S7 and S8 is ON, the voltage is $-4V_{dc}/15$ across the load.

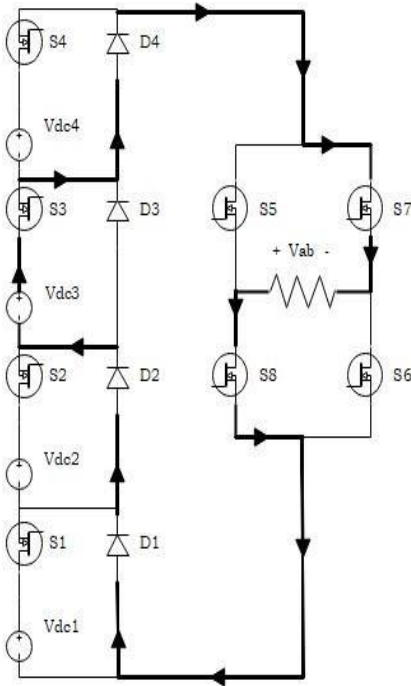


Fig 23. Mode 20

Mode 22:

Switch S2, S3, S7 and S8 is ON, the voltage is $-6V_{dc}/15$ across the load.

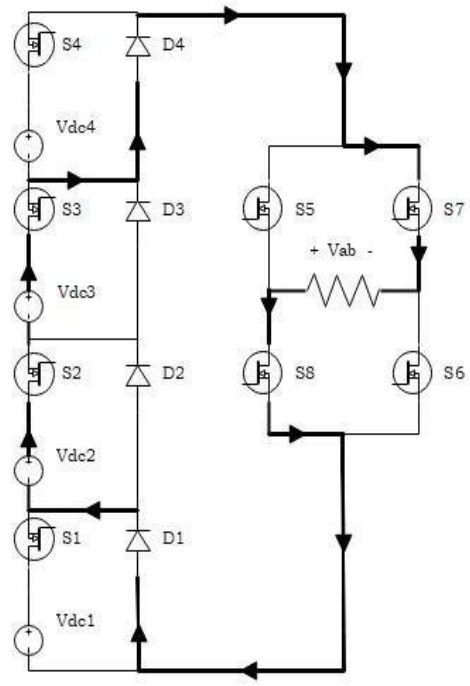


Fig 25. Mode 22

Mode 21:

Switch S1, S3, S7 and S8 is ON, the voltage is $-5V_{dc}/15$ across the load.

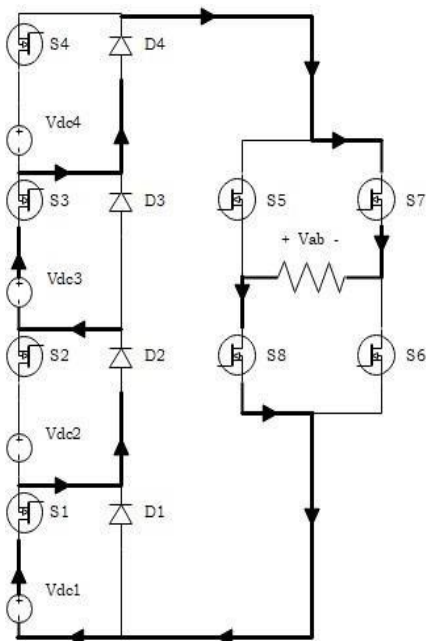


Fig 24. Mode 21

Mode 23:

Switch S1, S2, S3, S7 and S8 is ON, the voltage is $-7V_{dc}/15$ across the load.

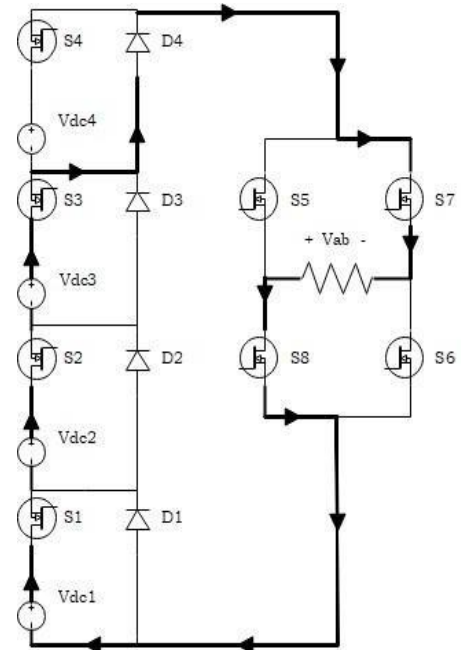


Fig 26. Mode 23

Mode 24:

Switch S4, S7 and S8 is ON, the voltage is $-8V_{dc}/15$ across the load.

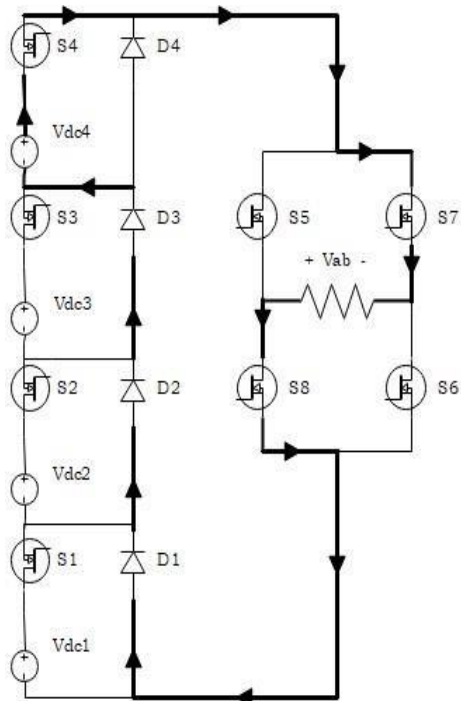


Fig 27. Mode 24

Mode 26:

Switch S2, S4, S7 and S8 is ON, the voltage is $-10V_{dc}/15$ across the load.

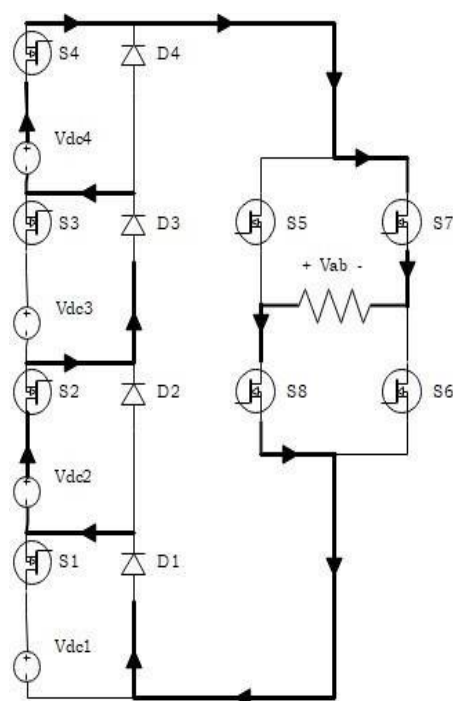


Fig 29. Mode 26

Mode 25:

Switch S1, S4, S7 and S8 is ON, the voltage is $-9V_{dc}/15$ across the load.

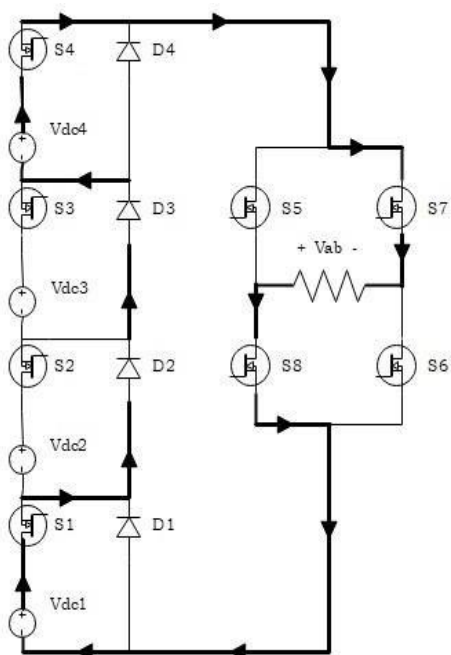


Fig 28. Mode 25

Mode 27:

Switch S1, S2, S4, S7 and S8 is ON, the voltage is $-11V_{dc}/15$ across the load.

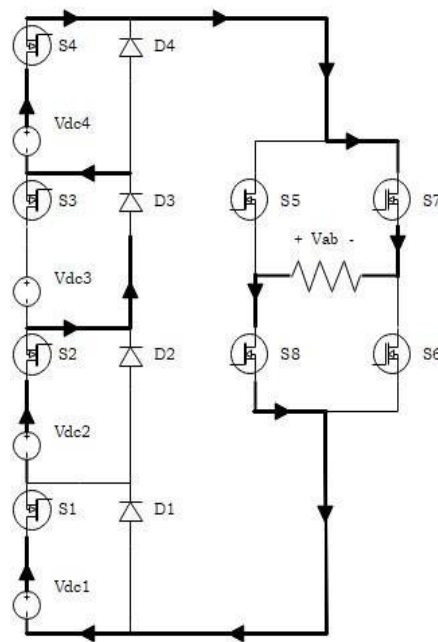


Fig 30. Mode 27

Mode 28:

Switch S3, S4, S7 and S8 is ON, the voltage is $-12V_{dc}/15$ across the load.

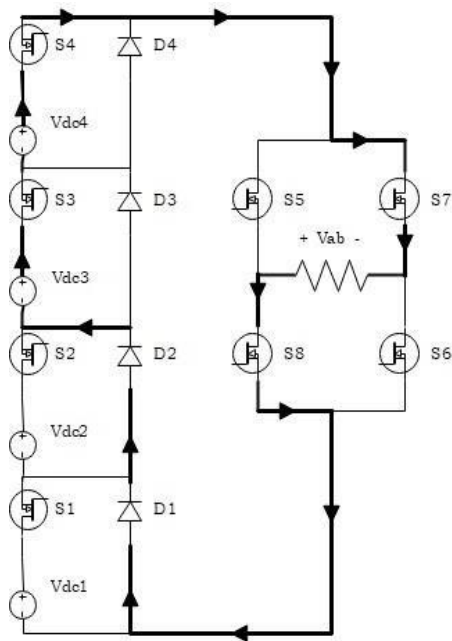


Fig 31. Mode 28

Mode 30:

Switch S2, S3, S4, S7 and S8 is ON, the voltage is $-14V_{dc}/15$ across the load.

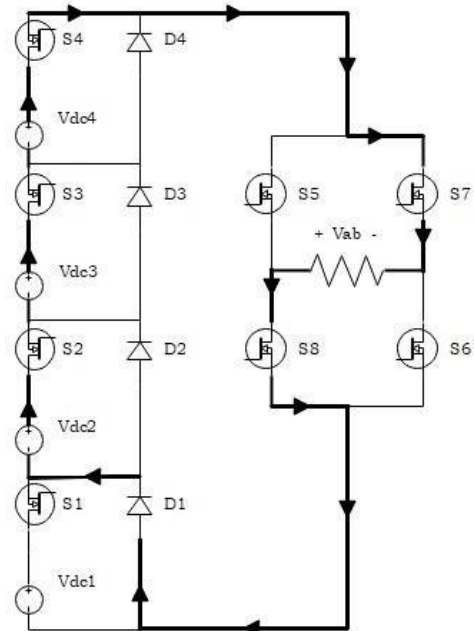


Fig 33. Mode 30

Mode 29:

Switch S1, S3, S4, S7 and S8 is ON, the voltage is $-13V_{dc}/15$ across the load.

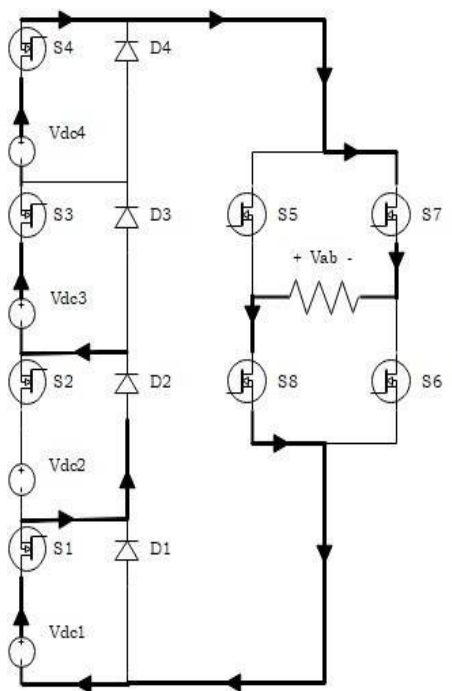


Fig 32. Mode 29

Mode 31:

Switch S1, S2, S3, S4, S7 and S8 is ON, the voltage is negative maximum $-V_{dc}$ across the load.

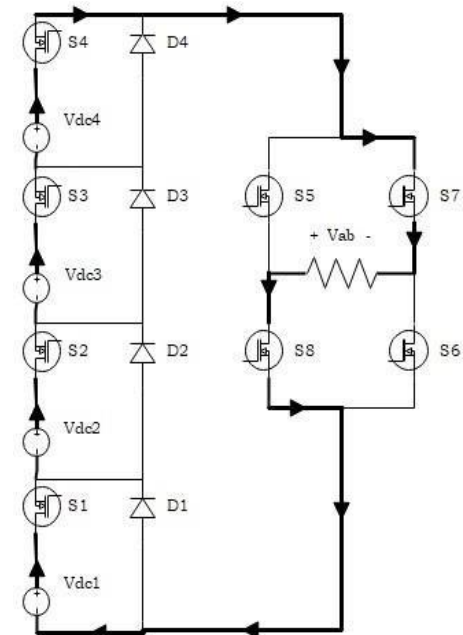


Fig 34. Mode 31

4. Modulation Technique

The pulse width modulation (PWM) uses a fixed DC input voltage which is given to the inverter and produces a controlled AC output voltage by adjusting ON-OFF periods of inverter components which can be exercised as a control for the output voltage within the inverter itself.

5. Phase Disposition Pulse Width Modulation

This is a level shifted multiple carrier pulse width modulation technique with all carrier signals in same phase.

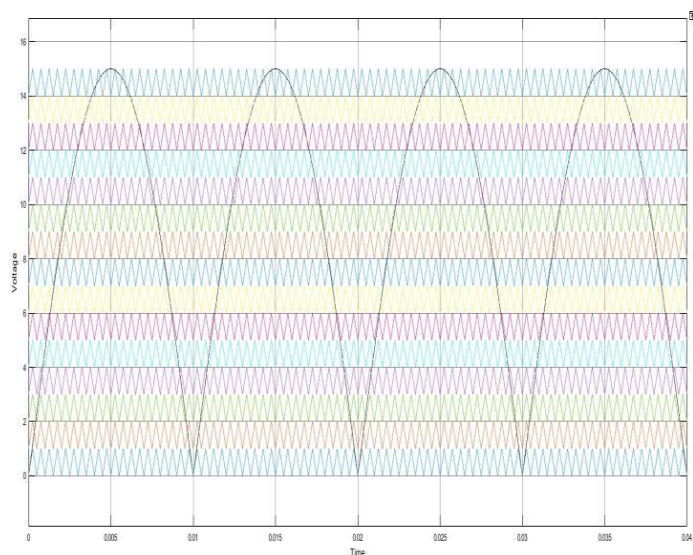


Fig 35. PD-PWM Technique

The reference signal is a sinusoidal wave of frequency 50Hz which is compared with triangular carrier waves of frequency 2Khz. The resultant output acts as gate signals for the MOSFETS.

6. Simulation and Results

The circuit diagram simulated in MATLAB is shown in Fig. 36.

The PWM control signals are generated in the subsystem block.

The switching pulses given for the switches S1, S2, S3 and S4 respectively is shown in Fig. 38.

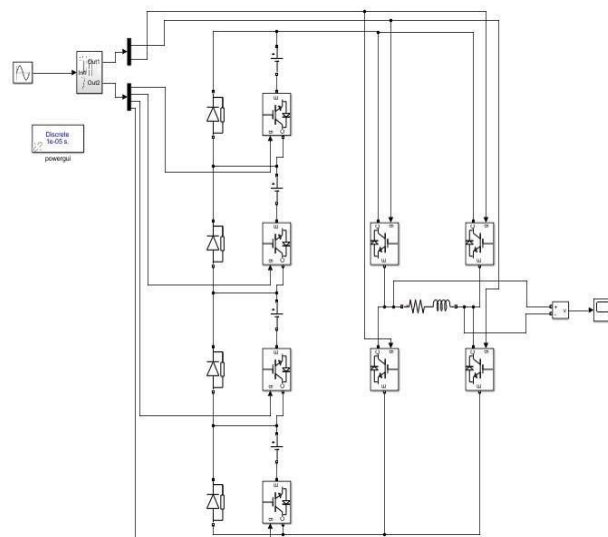


Fig 36. MATLAB Circuit Diagram

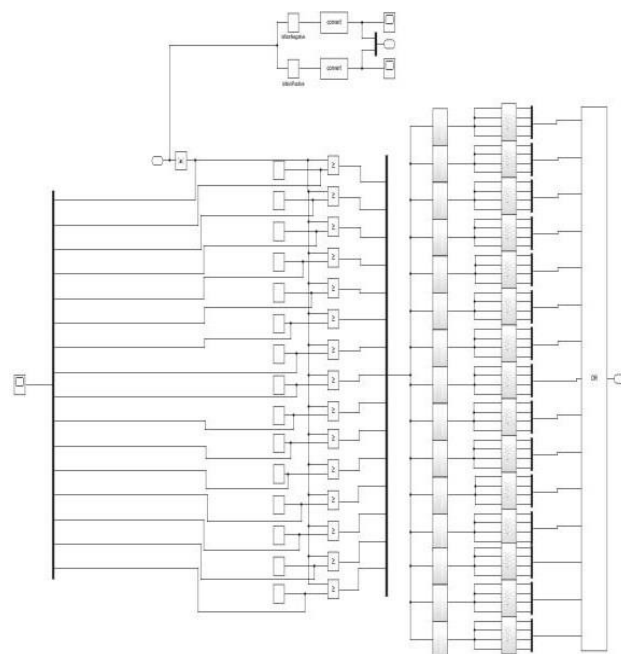


Fig 37. Subsystem Block

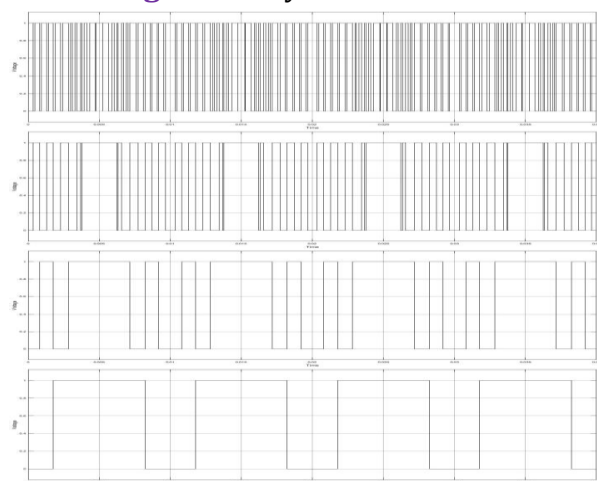


Fig 38. Switching Pulses for S1, S2, S3 and S4

The switching pulses for H-Bridge is shown in Fig. 39.

The circuit is simulated in MATLAB for different loads like R load of 400Ω and RL load of $400\Omega, 20\text{mH}$. The results obtained for R and RL

load are shown in Fig. 40 and Fig. 41 respectively.

The THD analysis for both the loads are observed and analysed to see the effects of change in loading which are shown in Fig. 42 and Fig. 43.

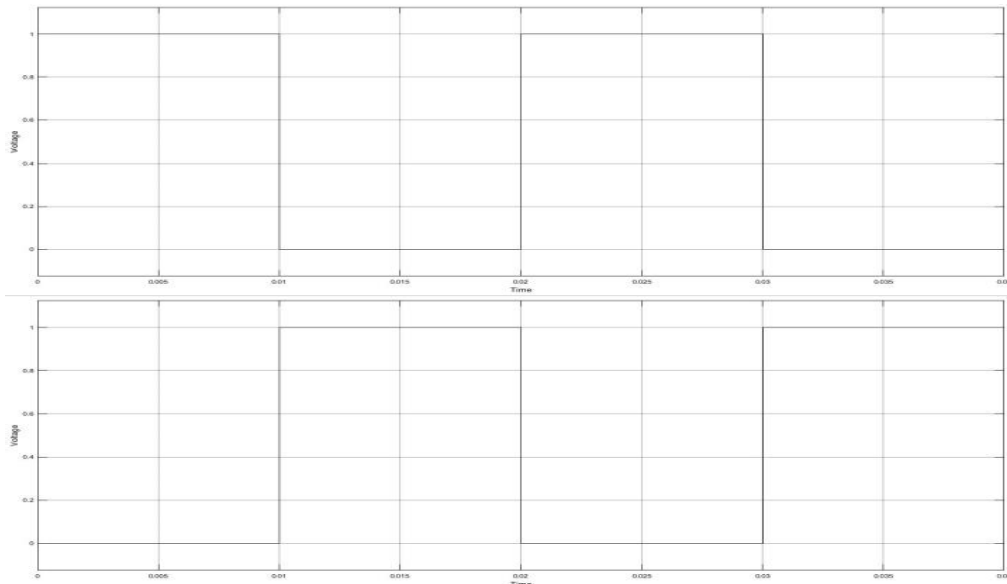


Fig 36. MATLAB Circuit Diagram

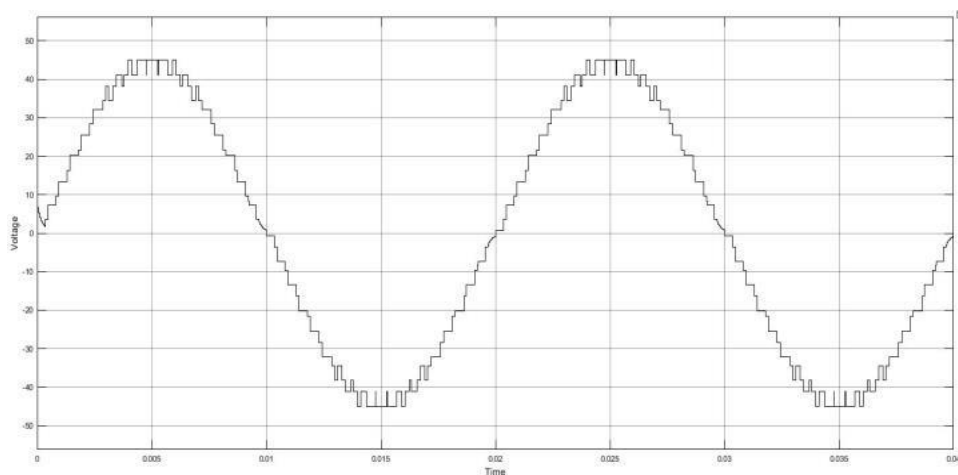


Fig 40. Voltage Waveform for R-Load

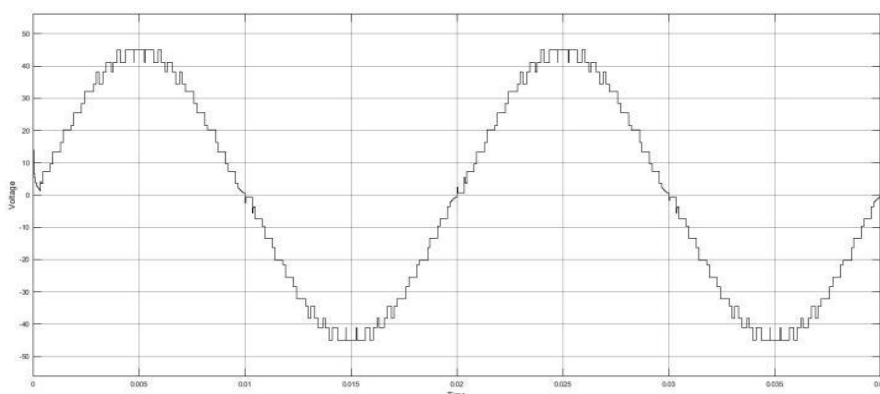


Fig 41. Voltage Waveform for RL-Load

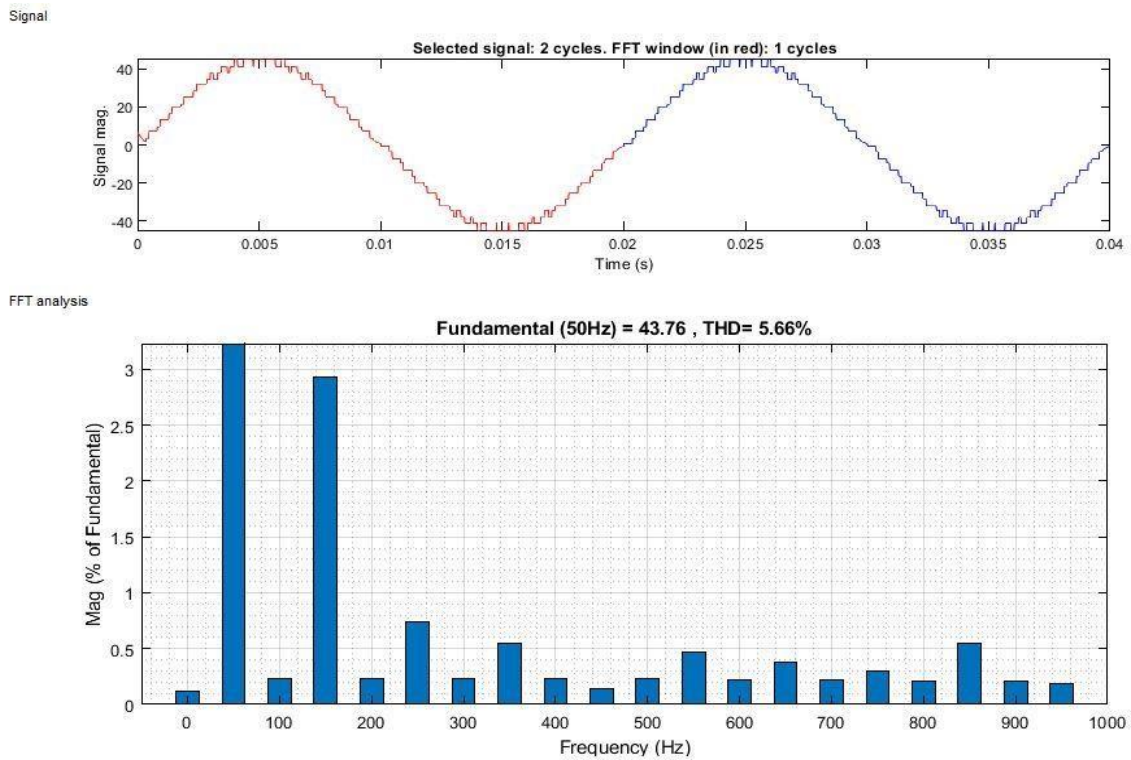


Fig 42. Voltage THD for R-Load

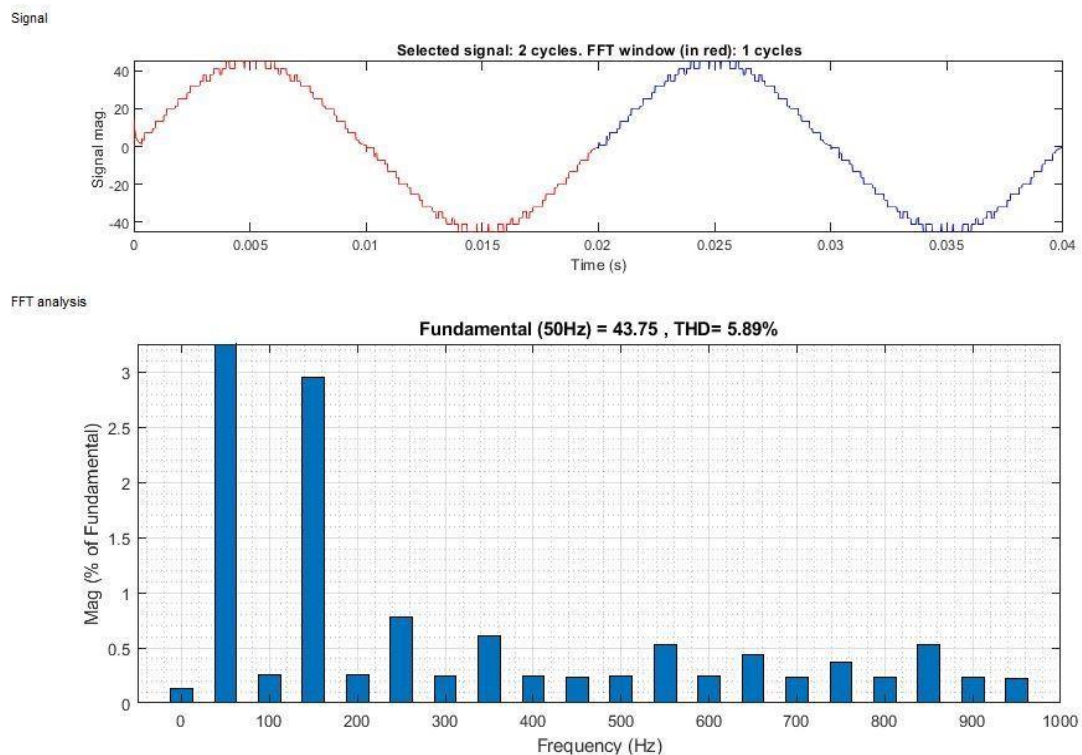


Fig 43. Voltage THD for RL-Load

7. Conclusion

The proposed multilevel inverter with reduced number of switches can be implemented for medium and high-power industrial applications. The basic operation of

the proposed MLI topology and the generation of required voltage level has been explained. The effective reduction of THD is achieved without using any filter in the circuit. The PD-PWM switching technique is simulated in

MATLAB/SIMULINK for various loads like R and RL.

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